INVESTIGATION INTO SOLDER JOINT FAILURE IN PORTABLE ELECTRONICS SUBJECTED TO DROP IMPACT

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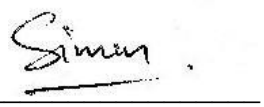
2012

DECLARATION

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.



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Summary

This thesis describes an investigation into the failure of solder joints – the critical interconnections between electronic components and printed circuit boards (PCBs) – as a consequence of dynamic loads caused by drop impacts of portable electronic devices. The research involves the development of new experimental methods, characterization of solder joint fatigue failure under dynamic loading, and the development and validation of a methodology for predicting solder joint failure under drop impact.

Experiments were performed to monitor the crack growth in a single solder joint during drop testing of a portable electronic device, in order to gain insights into how failure occurs under field use conditions. Crack growth tracking was accomplished using high-resolution and high-speed resistivity measurements, and a unique specimen design. Cracks were observed to advance with each drop or PCB bending cycle. The fatigue crack initiation phase is negligible, as cracks form in the first few load cycles under the high loading rates and amplitudes of typical drop impacts. The growth of a crack is gradual when it propagates in the bulk solder, but is accelerated or unstable when it propagates along intermetallic compound (IMC) layers that form the bond between solder joint and copper pad.

In the fatigue characterization study, dynamic bending tests on PCB assemblies were employed to subject solder joints to loads similar to those experienced in an actual portable device drop. Several parameters were investigated for their effect on fatigue failure, namely: 1) solder material; 2) pad finish; 3) PCB bending frequency; and 4) temperature. Several material systems were found to be highly

vulnerable to failure under drop impact. Low-silver solder joints (SAC101, SN100C) have excellent durability under dynamic loads, as indicated by high cycles-to-failure and consistent failure modes. Fatigue life decreases monotonically with frequency. High frequencies and large strains have a combined effect in reducing fatigue life and promoting brittle IMC failure. Low temperatures also reduce fatigue life, but only if the load amplitude is sufficiently high. These experiments provide a comprehensive description of fatigue characteristics needed for developing life prediction models. The effect of different load sequences on fatigue failure was also studied using the Palmgren-Miner rule to model cumulative damage caused by variable load histories; the cumulative damage parameter at failure was found to be less than unity for most of the load histories investigated.

Two fatigue models were developed using the fatigue characteristics identified. The first model condenses empirical fatigue S-N curves into a single equation by data fitting. The second model is based on a parameter that is a function of load amplitude and loading rate; this model collapses the S-N curves into a single unified characteristic curve. A drop impact life prediction methodology is then presented, and validated by comparison with several experimental cases.

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Chapter 1

Introduction and Literature Review

1.1 Introduction

Portable electronic devices have become essential tools for communication, work and entertainment today. As these devices are highly susceptible to drops, device manufacturers are faced with the challenge of ensuring that their products can survive drop impacts. This research focuses on impact-induced failure of *solder joints* that connect electronic components (or more specifically, integrated circuit (IC) *chip packages*) to the *printed circuit board* (PCB) of electronic devices. An example of a PCB with components mounted on it, termed a *board assembly*, is shown in Fig. 1.1. Because solder joints constitute both the mechanical bonds and electrical links between an IC package and a PCB, mechanical failure of solder joints will result in a loss of electrical functionality of the device. Figure 1.2 shows examples of solder joints that have developed cracks as a result of drop impact.

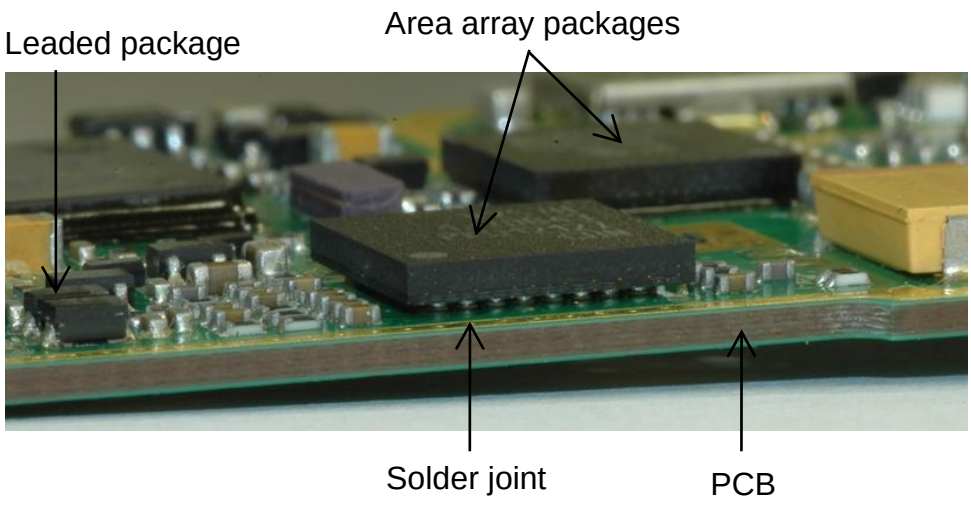


Figure 1.1: Board assembly of a mobile device.

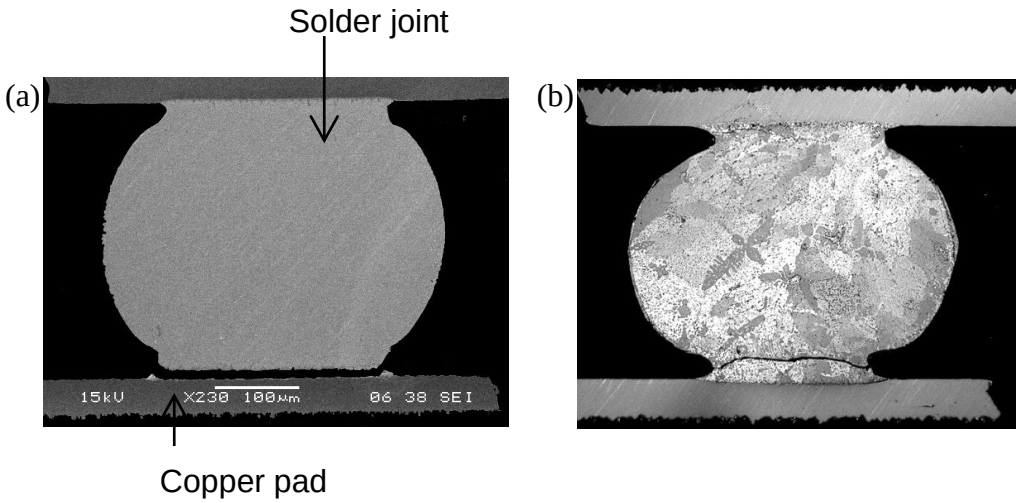


Figure 1.2: Cross-sections of failed solder ball joints. (a) Crack along IMC region between SAC305 (lead-free) solder joint and pad. (b) Crack in Sn-Pb bulk solder.

As mobile devices become smaller, thinner and lighter, and are equipped with ever increasing functionality, their board assemblies will require correspondingly greater interconnection densities. Today's smartphones, tablet PCs and advanced electronic gadgets invariably contain *area array* IC packages with high interconnection densities, such as those shown in Fig. 1.1. As the term implies, area array packages have solder joints arranged in an array over their surface area, thus permitting much higher interconnection densities than if the joints were arranged along the perimeter of the package, as is the case with older *leaded package* designs. Area array packages are particularly susceptible to impact-induced failure because they have stiff spherical *solder ball* joints that are poor in accommodating deformation. As area array interconnection densities increase and solder joints shrink, robustness against drop impact will be further impaired, because stresses in joints increase exponentially with a reduction in joint dimensions [1]. More information on the evolution of electronic package designs, with regard to accommodating higher interconnection densities can be found in

Appendix E [2], which is attached as a reference to serve as a general introduction to the field of electronic packaging.

Further compounding the drop impact problem is the industry-wide adoption of new lead-free solders, driven by the Restriction of Hazardous Substances Directive (RoHS) which came into force in 2006 and banned the use of established tin-lead solders in consumer electronics. Several lead-free solder materials which performed well under *thermal cycling* loading were observed to be extremely fragile under the dynamic loads caused by drop impact. Figure 1.2(a) shows an example of brittle failure of a lead-free solder joint resulting from drop impact. A crack has developed along the *intermetallic compounds* (IMC) that form the bond between solder ball and pad; the brittle crack growth caused the joint to fail within a few drops. In contrast, the bulk solder crack in the tin-lead solder joint of Fig. 1.2(b) requires many more drops to develop.

A drop impact of a mobile phone is captured in the high speed camera sequence in Fig. 1.3, where the phone strikes a rigid surface at an impact velocity gained during its fall from a height. Upon impact, a large portion of the kinetic energy is converted into vibrational energy due to dynamic bending of flexible elements that constitute the device, such as the device casing and board assembly. A very small portion of the board assembly's vibrational energy is converted into plastic work and work-of-fracture associated with damage and crack formation in the solder joints. The mechanics of solder joint deformation caused by PCB bending is illustrated by the finite element plot in Fig. 1.4, where joints at the edge of the component experience high stresses and strains due to a difference in the bending

curvature between the PCB and the component. Multiple stress/strain cycles over a series of drops induce fatigue damage in the solder joint. Figure 1.5 shows fatigue striations on the fracture surface of a joint which has failed after several drops, where each striation typifies the incremental crack advance during a loading cycle. Crack growth may also be catastrophic as a result of brittle IMC failure – as shown earlier in Fig. 1.2(a) – depending on the loading conditions and materials that compose the solder joint.

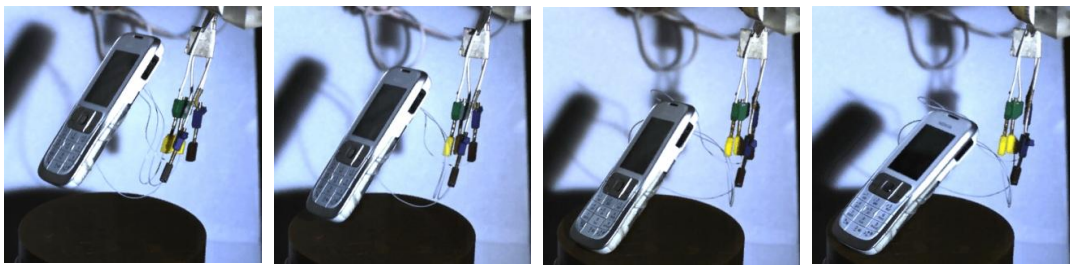


Figure 1.3: High speed video images of drop impact of mobile phone.

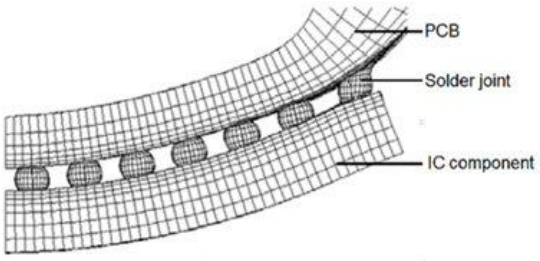


Figure 1.4: Finite element plot showing effect of PCB bending on solder joint deformation.

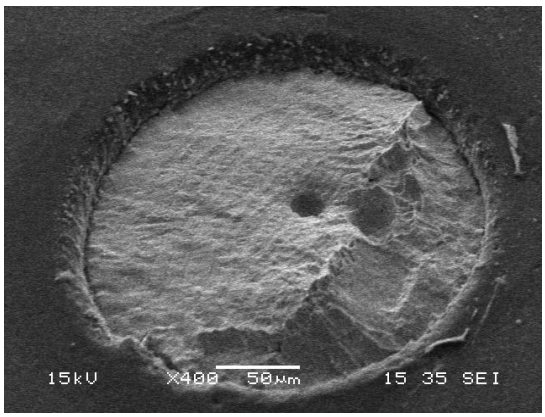


Figure 1.5: Striations on fracture surface of a joint which has failed under drop impact.

1.2 Research Gaps

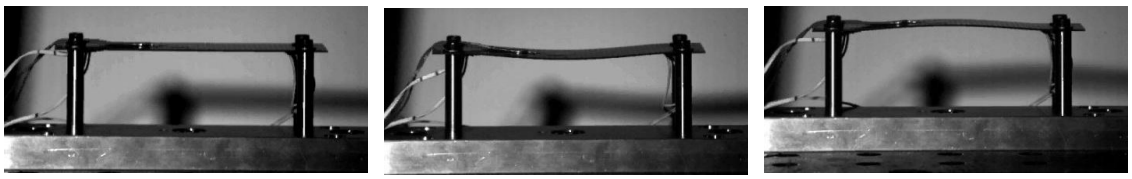
1) Lack of effective tools for evaluating solder joint robustness against drop impact

Given the rapid changes in designs, materials and components of portable electronic devices, it is important to have tools which not only allow quick assessments of solder joint robustness, but which also reflect field use conditions. An effective test method is one which reproduces, in a controllable manner, the high loading rates associated with dynamic structural responses to mechanical shock. This is because high strain rates increase the plastic flow stress in the solder and promote brittle failures which would otherwise not occur under slower loading rates. While the product drop test (or system-level test) shown in Fig. 1.3 reproduces the most realistic field conditions, such a test can only be performed after the device has been manufactured. A product drop test is also not suitable for controlled studies of various parameters that may affect robustness against drop impact. Thus, there is a need for *board-level tests* and *component-level tests* which can be used for materials and component evaluation prior to or during manufacture.

In a board-level test, shock accelerations, impact forces or bending loads are applied to a board assembly intended to represent the PCB assembly of a mobile device. An example of a board-level test is the JEDEC 22-B111 [3] drop test shown in Fig. 1.6(a). This standard industry drop test has been used primarily for comparing the robustness of various package designs and solder materials [4,5]. The main disadvantage of the standard drop test is that it prescribes only a half-sine shock pulse as the loading parameter; the cyclic loading that results from this shock pulse comprises a unique combination of bending amplitudes and

frequencies, shown in Fig. 1.6(b). Because variations in PCB materials and deviations of the shock pulse from the ideal half-sine profile can produce very different cyclic bending load histories, it is difficult to perform accurate comparisons across various drop test setups. In addition, the load history in a standard drop test is very different from that which may be encountered in product drop tests.

(a)



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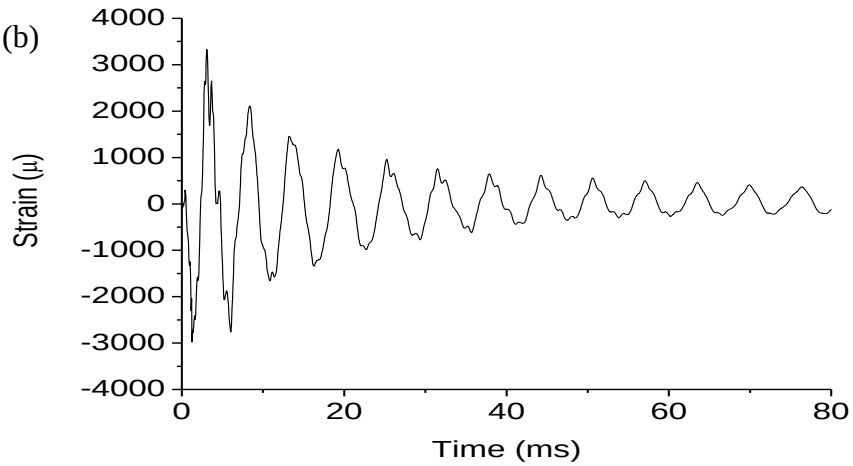
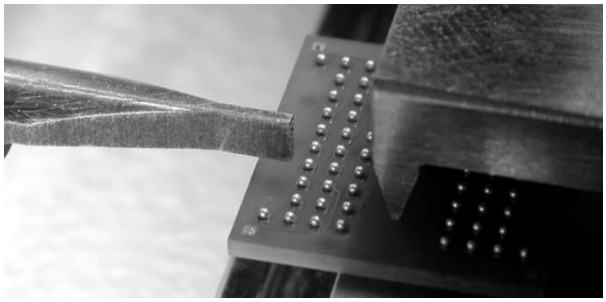


Figure 1.6: (a) High speed video sequence of JEDEC board level drop test showing dynamic bending of the board assembly after drop impact. (b) Bending strain load history.

In a component-level test, loads are applied directly to solder balls mounted on the pads of a component or package substrate. A high-speed ball shear test (Instron Micro Impactor) is shown in Fig. 1.7. Fig. 1.7(a) shows the experimental setup, while Fig. 1.7(b) shows a high speed video sequence of a shear test. Component-level tests offer the advantages of low sample costs and quick testing. However, because they apply predominantly shear loads, they cannot accurately reproduce

the state of loading on solder joints that results from PCB bending. Furthermore, while failures under drop impact result from fatigue under cyclic loading, failures in a high-speed shear test occur under monotonic loading.

(a)



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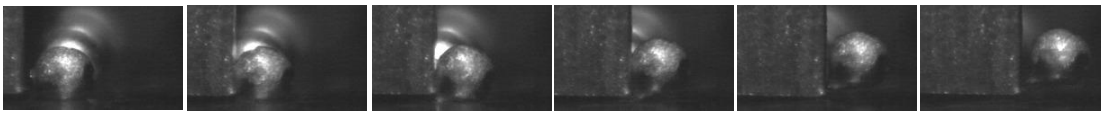


Figure 1.7: Component-level high speed shear. (a) Shearing blade next to ball-on-substrate samples (Instron Micro Impactor). (b) High speed video sequence of test.

2) Lack of information on solder joint failure under drop impact loading

Despite numerous studies in literature that report results on solder joint robustness in JEDEC drop tests [4-8], there remains a very limited understanding of the nature of low cycle fatigue that causes solder joint failure. Little information exists on fatigue damage development during drop impact, and factors that influence solder joint fatigue life and failure modes.

3) Absence of validated fatigue prediction methodologies for drop impact

Predictive fatigue models allow designers of portable electronic devices to estimate the robustness of electronic components used in their designs, prior to fabrication of the devices. A fatigue model for drop impact has to take into account the effects

of variable load amplitudes and frequencies that cause damage to solder joints. While cumulative fatigue damage models are well-established in other fields, none have been demonstrated to be applicable to solder joint failure under drop impact.

The research approach described in this thesis involves filling these research gaps. Firstly, experiments are performed to gain a qualitative understanding of solder joint failure under realistic loading conditions; novel experimental methods are devised in the process. Secondly, experiments are performed to characterize fatigue failure and quantify the effects of various parameters on fatigue life. The information obtained from the experiments is then integrated into a methodology for predicting solder joint failures under drop impact. Finally, validation experiments are performed to test the developed methodology.

1.3 Outline of Thesis

This thesis consists of six chapters. The ensuing sections of this chapter discuss prior work relevant to this research, via an extensive literature review. Chapter 2 introduces an experimental technique for tracking crack growth in solder joints. Chapter 3 describes an empirical study which provides insights into damage progression in solder joints when a portable electronic device is subjected to a series of drop impacts. Chapter 4 consists of a series of studies to investigate the influence of various parameters on fatigue failure of solder joints. Chapter 5 discusses the development of predictive fatigue models and a methodology for estimating damage caused by variable load histories. Finally, Chapter 6 presents a summary of the conclusions drawn from the research, and provides suggestions for future work.

1.4 Literature Review

1.4.1 Assessing solder joint robustness under drop impact

Date et al. [9] were the first to report on component level tests for evaluating the impact shear strengths of solder ball joints. They used a miniature pendulum tester, shown in Fig. 1.8(a), to determine the fracture energy of solder joints.

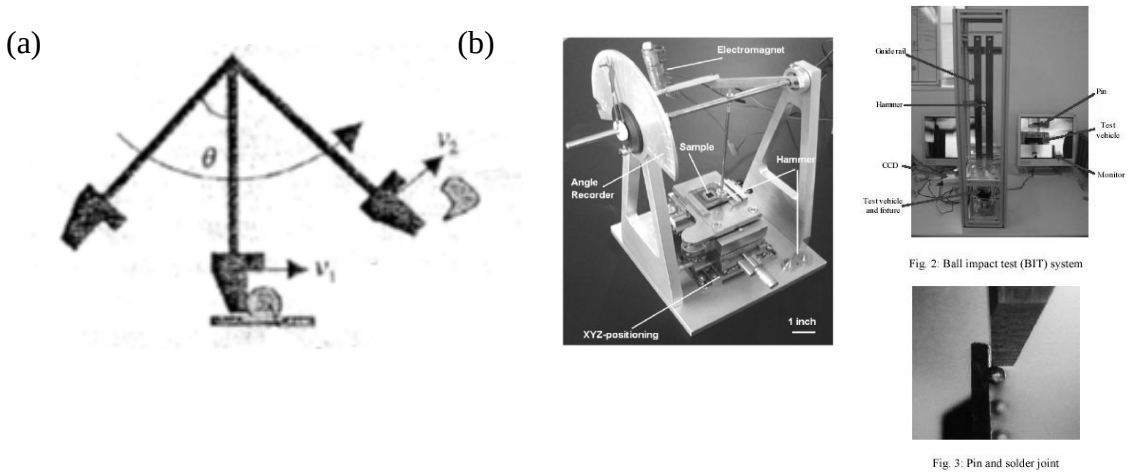


Figure 1.8: Impact shear test methods. (a) Pendulum tester of Date et al. [9] (b) Miniature Charpy impact tester of Ou et al. [10]. (c) Ball Impact Tester of Yeh et al. [11].

This early study was soon followed by several similar studies which also focused on assessing the shear strength of solder balls subjected to high loading rates. Ou et al. [10] developed a miniature Charpy tester, shown in Fig. 1.8(b), with which they tested a variety of lead-free solder joints, under various thermal aging conditions. From the observations of failure modes, they noted a ductile-to-brittle transition point as aging time increases. An interesting observation made is that impact toughness increases with aging time, despite the increasingly brittle failure modes. Yeh et al. [11] developed an impact shear device, shown in Fig. 1.8(c) whereby the shearing blade is dropped from a height onto the solder ball sample. Using this "Ball Impact Test" method, they performed a correlation study between the impact

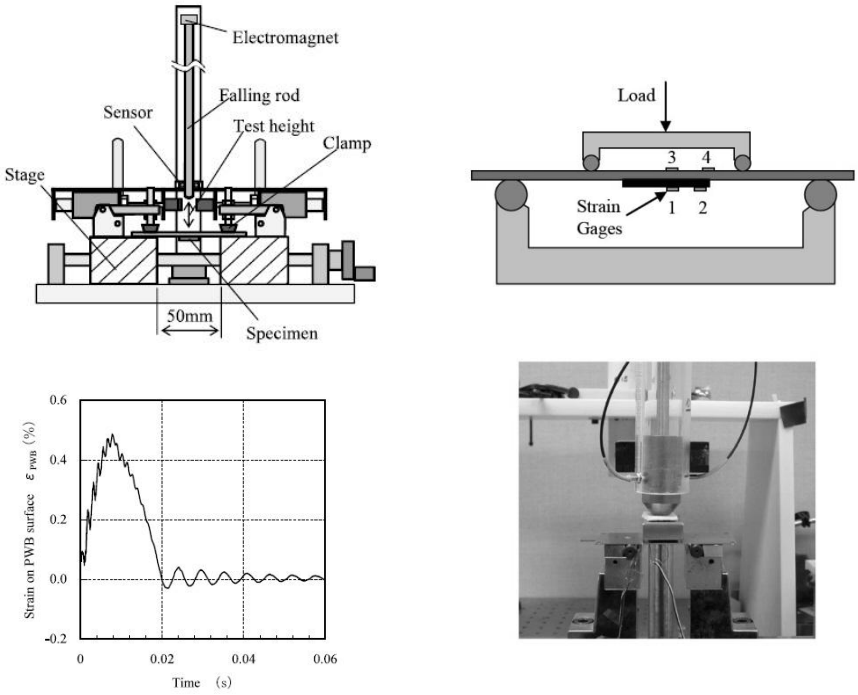
shear tests and JEDEC board level drop tests, for five solder alloys and two pad finishes [12]. They noted a correlation between impact energy/force in component level tests and board level drop impact performance for some of the materials tested. Song et al. [13] performed a comprehensive study of both high speed shear and pull tests on solder bumps using a motorized ball shear tester (Dage high speed shear tester). Results from these component level tests were also compared to results from board level drop tests. They noted that high-speed pull tests produced a higher percentage of brittle failure modes than high-speed shear tests. A correlation was observed between the proportion of ductile (or brittle) failures of joints in the component level tests, and the number of drops-to-failure in the board level tests. However, there was poor correlation between quantitative measures (energy and force from the component level tests), and number of drops-to-failure. Zhao et al. [14] performed similar impact shear and correlation studies using a spring-loaded impact shear tool (Instron Micro Impactor). They also concluded that a qualitative brittle failure index, obtained from observations of failure modes in component level tests, can be correlated to drops-to-failure in board-level tests.

The preceding component level testing studies discussed were motivated by the need for quick tests that could replace the JEDEC board level drop test, which was found to be time-consuming and costly. Every study that has attempted to correlate component level tests to board level tests has found that the shear fracture strength and fracture energy measurements exhibit poor correlation to drop impact performance. A key conclusion of these studies is that the observed failure modes in component level tests can be correlated with drop impact performance. However, converting observations of failure modes into a “percentage brittle

failure" quantity is very much subject to human interpretation. Difficulties in correlating high speed shear results to drop impact performance are due to several factors, namely: 1) differences in stress states created by shearing (component level tests) and PCB bending (drop tests); 2) monotonic failure in shear tests versus fatigue failure in drop tests; and 3) difficulties in identifying an impact shear speed that would provide a good correlation for a wide range of solder alloys and pad finishes.

Board-level tests allow much more realistic loading conditions to be applied to the solder joint, but are more costly due to the need to fabricate board assemblies; this contrasts with shear tests, which require only bumped components. Despite the existence of a standard board level test method (JEDEC), various studies have been performed to develop alternative board level test approaches. The key motivating factor for the development of new board level test methods is to improve the consistency, repeatability and speed of testing. These alternative test methods do not necessarily involve drops or shocks, but ultimately produce PCB bending at high frequencies and strain amplitudes. Yaguchi et al. [15] produced one of the earliest works on the reliability of solder joints under dynamic PCB bending. They used a tester which applied direct impact to a PCB using a falling mass, as shown in Fig. 1.9(a). Reiff and Bradley [16] proposed a similar test method, shown in Fig. 1.9(b), which involved a falling mass impacting a PCB indirectly through a four-point loading fixture. These falling mass test methods induce a single half-sine bending pulse instead of the multiple-cycle load history of the JEDEC test shown in Fig. 1.6(b). Therefore, the damage due to a single strain cycle can be studied. A

disadvantage of this method is that the bending frequency – being dependent on the PCB stiffness, support conditions and drop mass – is not easily specified.



(a) (b)

Figure 1.9: Board level tests using falling masses: (a) Impact bend test of Yaguchi et al [15]. (b) Four-point impact bend test of Reiff and Bradley [16].

Marjamaki et al. [17] and Mattila et al. [18] used electromagnetic shakers to apply high-amplitude and high-frequency bending to a board assembly. Since the acceleration limits of shakers are much lower than shock accelerations, the vibration tests were run near the resonant frequency of the mounted board assembly in order to achieve similar amplitude levels as those in drop impact. Ensuring repeatability is a challenge, because the board assembly vibration has to be maintained within a narrow frequency band for resonance to occur. Also, applying constant load amplitudes or single bending cycles is not possible owing to the ramp-up period of shakers; the damage resulting from a single cycle therefore cannot be studied via a shaker test. Novel shock tests which excite discrete PCB

bending cycles have also been suggested. Pringle et al. [19] proposed the use of shock tests with a prescribed trapezoidal shock pulse intended to induce a PCB response of several constant-amplitude half-sine bending pulses.

Seah et al. [20] developed a high-speed cyclic bend tester for applying high-speed and high-amplitude cyclic bending loads to PCB assemblies. The tester applies sinusoidal bending cycles at variable amplitudes and frequencies to a PCB assembly test vehicle. The tester is driven by a cam which has a motion profile that is limited to a small angle on the cam perimeter, with the remainder of the perimeter maintaining a dwell period. This cam design allows high bending frequencies to be applied without requiring prohibitively high motor speeds, and produces discrete bending cycles, thus facilitating the study of damage caused by individual amplitudes and frequencies present in complex load histories. The cyclic bend tester also significantly cuts the time needed for both the setup and running of board-level tests. This test method is used in the present research.

1.4.2 Life prediction modeling for drop impact

One of the earliest works involving modeling of the fatigue life of solder joints under complex load histories was presented by Barker et al. [21] in 1991. They proposed a method for predicting the life of solder joints under a combination of high-cycle vibrational fatigue and low-cycle thermal cycling fatigue, as illustrated in Fig. 1.10(a). The starting point of their unified methodology is experimental fatigue data plotted in the form of solder strain amplitude against cycles to failure, or S-N curves (Fig. 1.10(b)). The Palmgren-Miner Rule [22,23] is then used to superpose the effects of various load amplitudes, and generate a damage metric that represents the life consumed by the complex loading history.

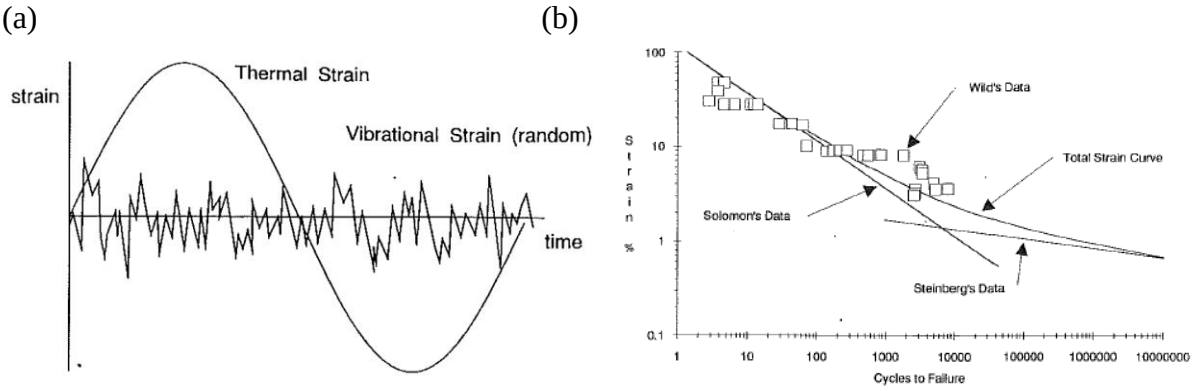


Figure 1.10: (a) Complex load history investigated by Barker et al. [21]. (b) Fatigue data on which their unified life prediction methodology is based.

Much of the existing literature relating to low cycle fatigue of solder joints addresses the problem of thermal cycling fatigue in solder joints, which involves strain rates in the order of $0.001s^{-1}$ to $0.01s^{-1}$, and test frequencies much lower than 1 Hz [24-27]. Kanchanomai et al. [24] studied the low-cycle fatigue behavior of lead-free solders using dogbone specimens, and performed an investigation on

crack propagation through various microstructural features (grains, phases, dendrites, voids) in bulk solder material. Erinc [25] studied the thermomechanical failure of lead solder joints on a Ni-Au interface; in particular, fatigue characterization of IMC interfaces was performed using lap shear specimens to obtain parameters for a cohesive zone damage model. Shi et al. [26] performed a low cycle fatigue study on the effects of temperature and frequency on failure of bulk eutectic SnPb solder. Test frequencies ranged from 0.0001 Hz to 1 Hz, while test temperatures ranged from -40°C to 150°C. They found that increased temperatures and lower frequencies result in a drop in fatigue life, owing to the fact that fatigue failure at these low strain rates are dominated by creep damage. Berriche et al. [27] studied the effects of hold time in strain-controlled fatigue tests, as well as the effects of ambient, wet, dry and CO_2 environments. They found that an increase in hold time reduces fatigue life, owing to the effects of creep.

More recently, Wong et al. [28] presented a study on fatigue life prediction of BGA lead-free solder joints, for the application of vibration of computer motherboards. S-N curves were generated using constant amplitude vibration tests, and validation of the Palmgren-Miner Rule was performed using random amplitude vibration tests. Lead-free solder joints were found to have a better high-cycle fatigue performance than solder joints containing lead; however, the performance is reversed for low-cycle fatigue. They also noted that damage estimates (or Miner's sums), are dominated by high strain components. Varghese and Dasgupta [29] presented a methodology, also based on the Palmgren-Miner Rule, for modeling damage caused by drop impacts. Pendulum impact tests, as shown in Fig. 1.11, were used to generate fatigue S-N data. However, the

methodology was not convincingly validated, because the validation tests used a setup that was identical to the one used to generate the S-N data. Wavelet analysis has also been suggested for decomposing transient drop impact waveforms into their constituent components. Lall et al. [30] proposed a similar failure modeling methodology, but their fatigue data was obtained from much less controllable drop impact tests. Validation was again performed under very similar test conditions as that used to generate the fatigue data; thus the general applicability of the methodology is not proven.

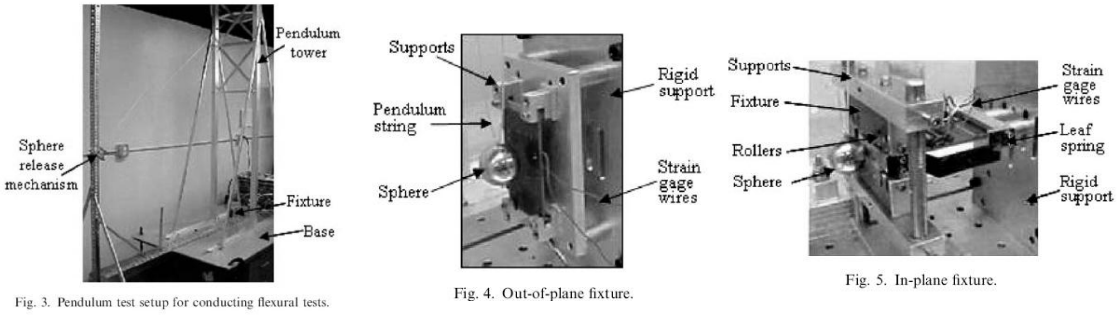


Fig. 3. Pendulum test setup for conducting flexural tests.

Fig. 4. Out-of-plane fixture.

Fig. 5. In-plane fixture.

Figure 1.11: Pendulum impact tests used in the life prediction methodology of Varghese and Dasgupta [29].

Several life prediction studies for drop impact have proposed the use of methods similar to thermal cycling fatigue prediction methods, such as the Coffin-Manson relation [31]. Syed et al. [32] proposed a model for predicting the drop impact life of board assemblies in JEDEC drop testing. The first plastic strain peak of the PCB shock response is used as the loading range parameter in the fatigue model. The model is therefore only able to predict the drop impact life for the same experimental setup and sample used to generate the model, and would not be applicable to other situations (e.g. product drop impacts), which have completely different board assemblies, support conditions and load histories. A life prediction

methodology for drop impact requires a more sophisticated treatment than that for thermal cycling, owing to the more complex load histories involved. In contrast, thermal cycling fatigue methodologies typically assume loading histories of constant amplitude and frequency. Syed et al. [33] also proposed the use of an accumulated plastic strain metric, obtained from computational simulations, to represent damage in solder joints resulting from PCB bending. Figure 1.12 shows the increase in accumulated plastic strain with bending cycles in a solder joint. The implicit assumption underlying this method is that the accumulated plastic strain is a representation of the actual damage in the solder joint; in reality, the formation of cracks may prevent the development of such high levels of plastic strain.

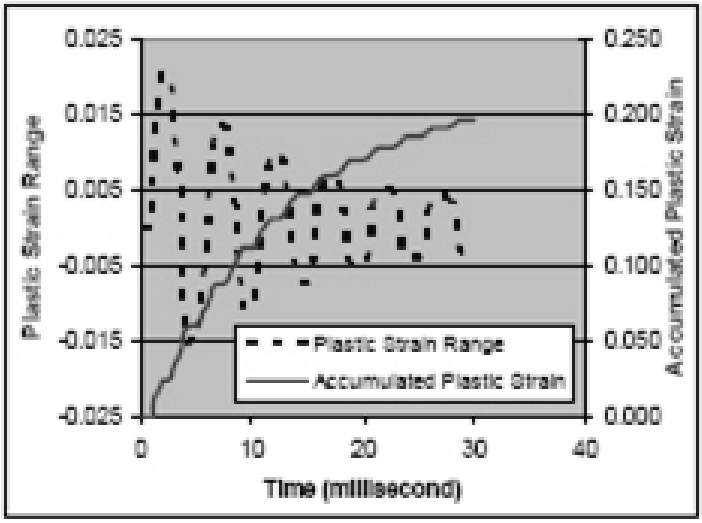


Figure 1.12: Accumulated plastic strain metric proposed by Syed et al. [33].

1.4.3 Advances in lead-free solder materials

A major area of research in electronic packaging is the development of reliable lead-free solder materials. This section reviews several studies which focus on the robustness of the bond between a solder joint and a pad under high strain rate loading. Amagai [34] performed a very comprehensive and in-depth study of the effect of a wide range of nano-particles, also termed dopants, in reducing IMC growth in solder joints on bare copper pads. Electron microscopy was used to investigate IMC thickness and grain size for various solder alloys and reflow conditions. The strength of the joints was evaluated using high-speed pull and drop tests, and the study concluded that elements to the left of Cu in the periodic table (Co, Ni, Pt) are effective in reducing IMC growth and improving drop impact performance.

Tanaka et al. [35] performed an investigation into the drop impact performance of tin-silver-copper (SAC) solder alloys with and without nickel (Ni) dopants. Thinner IMC layers and improved drop performance were observed for Ni-doped solder joints. Figures 1.13(a) and 1.13(b) show the effect of Ni in limiting the growth of the IMC region adjacent to the solder pad. The elemental analysis corresponding to Fig. 1.13(c) shows that nickel is concentrated at the board pad. A theory proposed in their study is that drop impact performance improvement is due to a reduction in the stress mismatch between the Cu_3Sn and Cu_6Sn_5 compounds in the IMC region. The Ni substituting for Cu in the Cu_6Sn_5 structure relieves some of the stress mismatch. However, while the study claims that the drop impact performance improvement is due to the Ni dopants, it is not certain if the

improvement is actually because of a lower silver content of the doped solder material, which would result in a lower plastic flow stress [36].

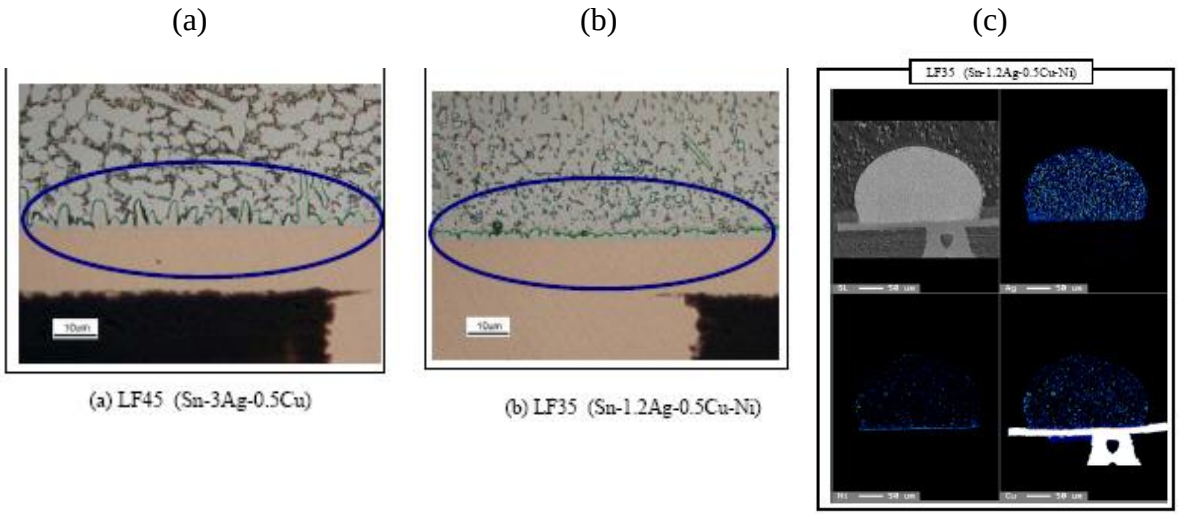


Figure 1.13: Differences in IMC microstructure between (a) tin-silver-copper (SAC) solder joint, and (b) SAC joint with Ni dopants. (c) Elemental analysis showing concentration of Ni at the solder pad [35].

Lee et al. [37] performed a study on the fracture process in solder joints with cobalt dopants, using quasi-static ball shear tests. The shear strength was found to increase with %Co up to a point, after which the strength decreased. An interesting explanation for this trend is that for lower concentrations of Co, the IMCs form obstacles in the fracture path, but at higher concentrations, they are sites for initiation of fracture. Figure 1.14 shows the microstructures of the IMC regions for various Co concentrations.

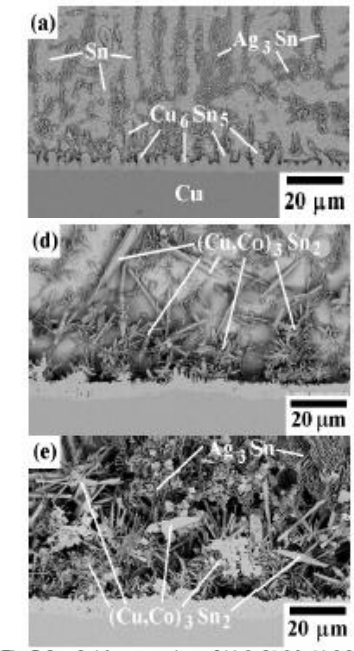


Fig. 7. Interfacial cross-sections of (a) 0, (b) 0.1, (c) 0.5, (d) 1.0, and (e) 2.0 wt. % Co-reinforced Sn-3.5Ag on Cu.

Figure 1.14: IMC structures formed for various amounts of Co addition, from Lee et al. [37]

1.4.4 Product drop tests

Lim et al. [38] and Seah et al. [39] performed instrumented drop tests on a variety of portable electronic devices. Examples of mobile devices tested are shown in Fig. 1.15. The drop tests were part of a survey to gather information on the types and levels of mechanical loads that are experienced by the electronic components of mobile devices.

Figure 1.15: Several mobile devices tested in product drop test survey [39].

These responses were measured using miniature strain gauges and accelerometers mounted on the PCB assembly. Strain gauges were mounted on the PCB adjacent to components to measure the degree of PCB bending. In-plane and out-of-plane (with respect to the PCB plane) accelerometers were mounted on the components of several devices to measure the inertial loading on solder joints. The directions of measurement are shown in Fig. 1.16. Figure 1.17 shows examples of sensors mounted on the board assembly.

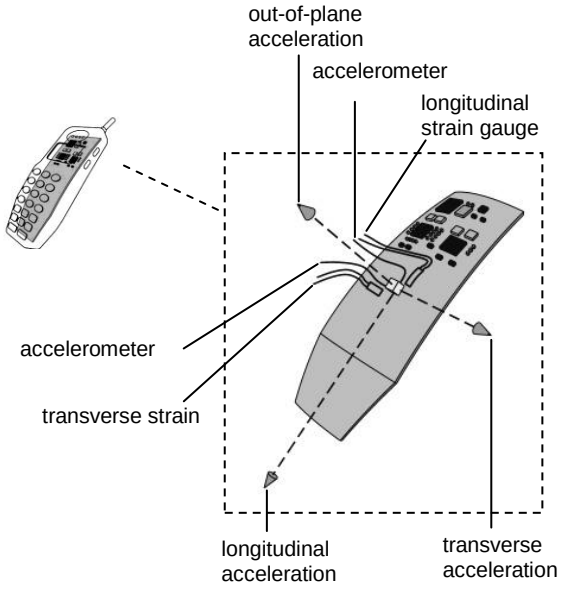
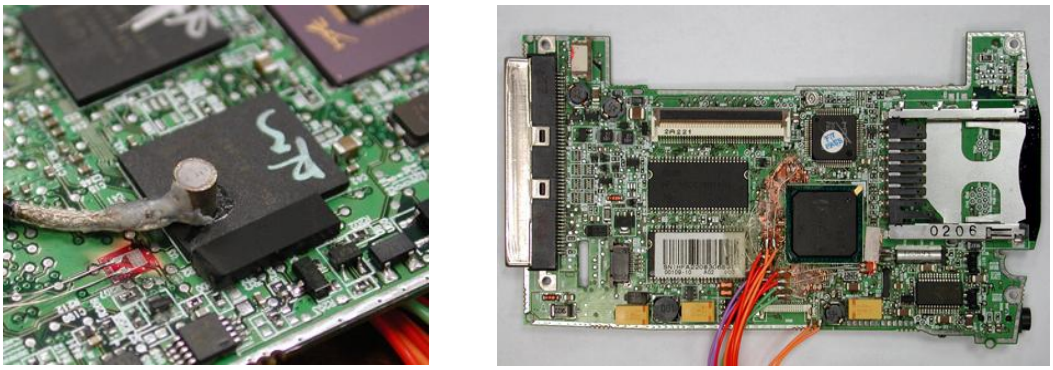


Figure 1.16: Board assembly showing measurement directions of sensors [40].



(a) (b)

Figure 1.17: Sensor mounting for product test. (a) Strain gauge and accelerometer mounted on board assembly. (b) Strain gauges around package, with lead wires connected to gauges [40].

Each product was subjected to drops from a height of 1 metre onto a load cell, which measures the impact force and triggers data capture. Figure 1.18(a) illustrates several drop orientations tested. Orientation control is achieved using a specially-designed gripper [41], shown in Fig. 1.18(b), that maintains the product's orientation through much of the free fall and releases the product just before impact, thus ensuring that impact occurs in the desired orientation.

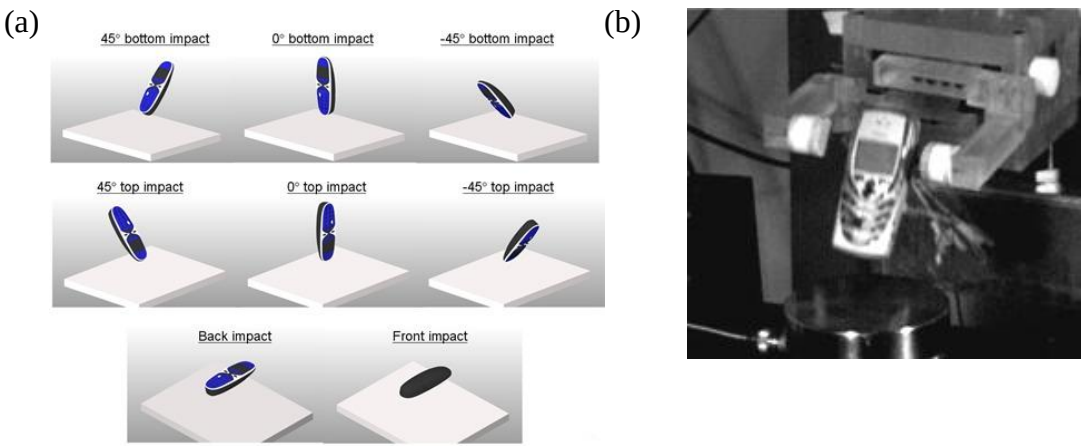


Figure 1.18: Product drop test. (a) Orientations.
(b) Gripper that facilitates orientation control [38].

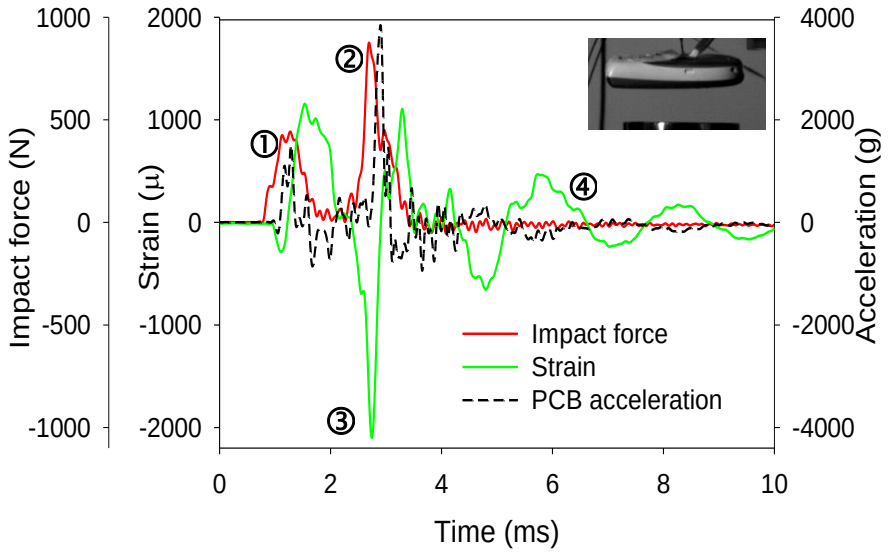


Figure 1.19: Measured responses for a flat orientation impact [38].

Figure 1.19 shows data captured (impact force, PCB strain and out-of-plane acceleration) during a mobile phone drop in a horizontal (flat) impact orientation. The impact force waveform has two major peaks ① and ②, corresponding to two impacts on the phone body. Due to the horizontal impact orientation, the phone experienced a light impact ① on one of its edges or corners, before a more severe impact ② over the entire face of the phone. Note the severe spike in PCB strain ③ having a magnitude of approximately 2000μ. The PCB continues to flex dynamically beyond the duration of impact contact, when the product has rebounded into the air, as indicated by ④. Figure 1.20(a) shows an example of PCB strains captured during the drop of a mobile phone at an angled orientation [39]. The strains correspond to the four board locations shown in Fig. 1.20(b). Two strain spikes, labelled ① and ②, interrupted by a short pause, can be observed: ① is generated by the first impact on the phone, which causes the phone to rebound and rotate in the air; and ② is generated by a second impact at the other end of the phone due to its rotation.

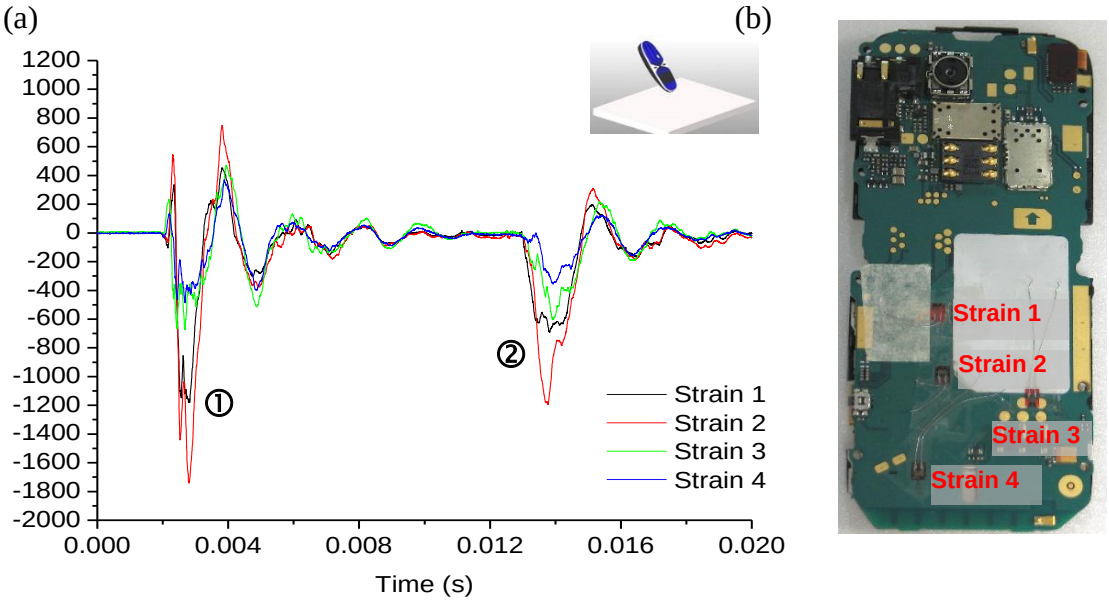


Figure 1.20: Impact at 45° orientation. (a) Strain gauge measurements. (b) Strain gauge locations [39].

Several modes of mechanical responses can be identified from the product tests: 1) bending of the PCB assembly causing differential flexing between the PCB and the IC component, with resulting deformation of the interconnecting solder joints; and 2) high accelerations of components resulting in inertial loading on solder joints. Board-level experiments designed to isolate and study the effect of bending and inertial loading on solder joint failure are discussed in the next section.

1.4.5 Physics of solder joint failure in drop impact

Wong et al. [42] investigated the effect of PCB bending and inertial loading on solder joint failure. To study the effect of PCB bending, instrumented drop tests were performed on board assemblies supported at four corners on a shock test fixture. During the tests, a high-speed data logger was used to monitor the dynamic bending strains in the PCB and the electrical connectivity of daisy-chained solder joints. The experimental setup is shown in Fig. 1.21.

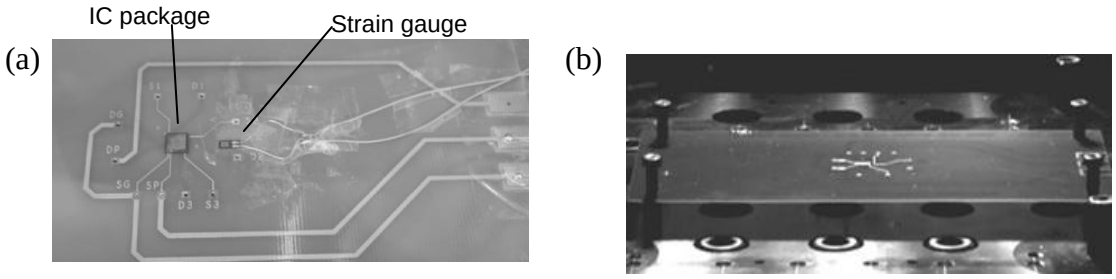


Figure 1.21: Board level drop test setup, with (a) strain gauge mounted near component; and (b) board mounted on shock test fixture, from Wong et al. [42].

Figure 1.22 shows the variation of PCB strain and electrical resistance with time in the drop where electrical failure occurs. The PCB strain waveform consists of two superimposed vibration mode components, namely a fundamental mode with a

period of approximately 5ms, and a higher frequency bending mode with a period of 0.8ms. Immediately prior to impact at time t=2ms, the daisy chain was still electrically intact; this is indicated by a low electrical resistance level. The impact shock sets the PCB into dynamic oscillations, and an open circuit occurs at t=3ms, indicated by the almost vertical jump in electrical resistance. The plateaus in the electrical resistance curve indicate the maximum limit of the resistance measurement, or an open circuit. Subsequently, there is intermittent closing and opening of the electrical circuit, corresponding to the peaks and troughs of the higher frequency bending component. This correspondence between the electrical connectivity and bending strain suggests that PCB bending, and not direct inertial shocks, causes solder joint failure during drop impact.

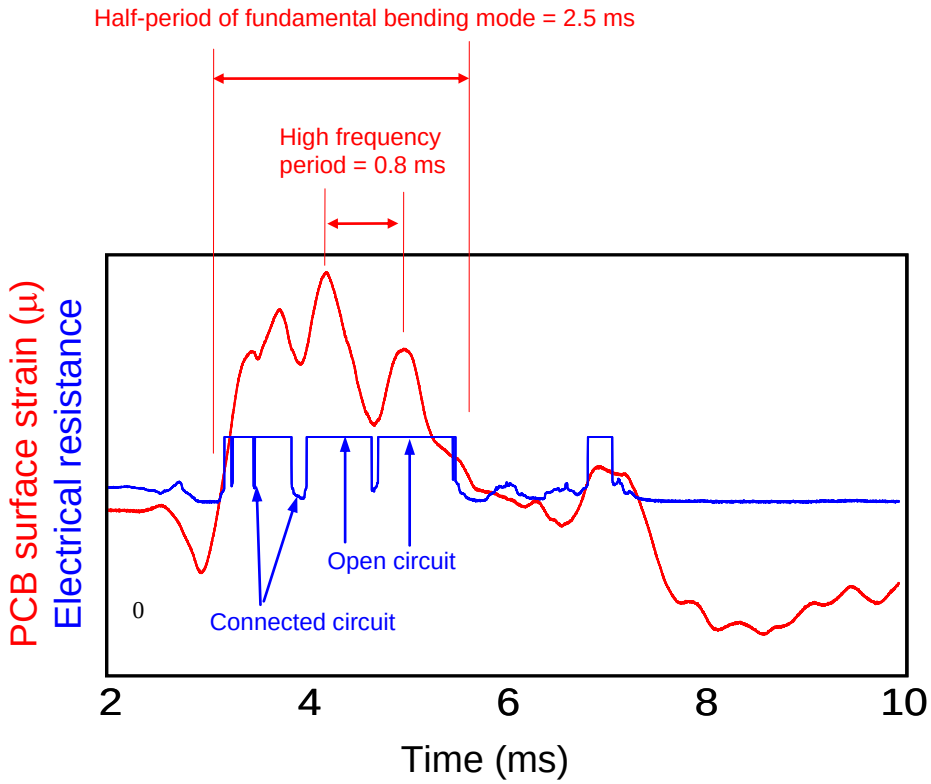


Figure 1.22: PCB strain and electrical resistance waveforms from a board level shock test [42].

A simple experiment was performed to study the effect of inertial loading. This experiment was designed to minimize PCB bending in a shock test, and is shown in Fig. 1.23. The board assembly is cut to a size slightly larger than the package and attached by adhesive to the underside of a rigid extension that overhangs the shock table. An inertial mass is bonded to the surface of the component. The attached steel plate increases the component mass by sevenfold. The overhanging extension is rigid enough to prevent flexing of itself or the PCB, so as to ensure that the loading on the solder joints is purely inertial. A shock pulse of 3000G amplitude and 0.5 ms duration is then applied to the shock table. During setup tests, a miniature accelerometer (APTech AP19) is used to verify that the acceleration pulses measured at the shock table and at the top of the overhanging extension are similar, and that the extension is sufficiently rigid. Even with the increased component mass, the electrical connectivity remains intact at the end of the prescribed number of tests (30 drops), whereas a free flexing board fails at approximately 10 drops.

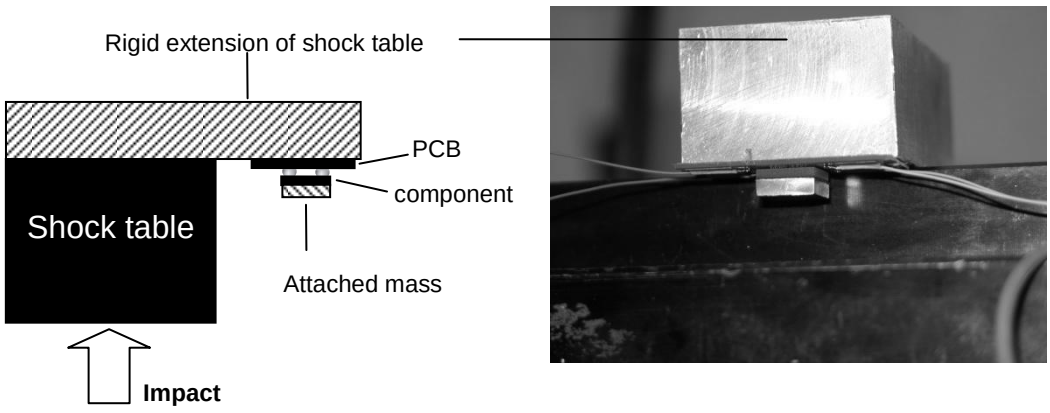


Figure 1.23: Experiment to investigate inertia loading [42].

1.4.6 Analytical solutions for solder joint stresses

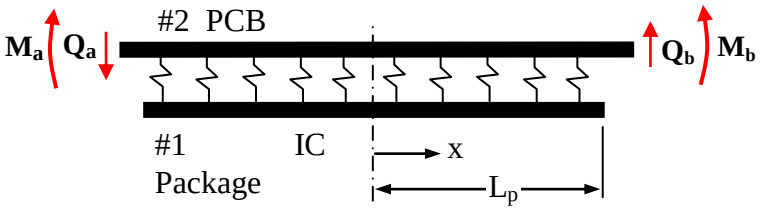


Figure 1.24: Analytical model of Wong et al. [43].

Wong et al. [43] developed an analytical model for determining solder stresses under conditions of PCB bending. The solder joints are modeled as a layer of springs between the PCB and component, and the PCB and component are modeled as linear elastic beams. The problem is therefore similar to that of a beam on an elastic foundation (Fig. 1.24). Using this model, stresses in the solder joints can be estimated for any combination of bending moments applied to the PCB near the edges of the component. The maximum stress in the solder joint at the edge of the component is given by

$$\max \sigma_p = \frac{k_a (M_a + M_b)}{4\alpha^2 D_2} \psi_1(u) + \frac{k_a (M_a - M_b)}{4\alpha^2 D_2} \psi_2(u)$$

where k_a is the axial stiffness of the each solder joint, α the composite stiffness of the PCB, defined by $4\alpha^4 = k_a/D_e$, k_a the axial stiffness of the solder joints, D_e the equivalent flexural stiffness of the PCB and package given by $1/D_e = 1/D_1 + 1/D_2$, where subscripts 1 and 2 denote the package and PCB respectively, and

$$\psi_1(u) = \frac{\sinh(2u) - \sin(2u)}{\sinh(2u) + \sin(2u)}$$

$$\psi_2(u) = \frac{\cosh(2u) - \cos(2u) - u[\sin(2u) + \sinh(2u)]}{u[\sin(2u) - \sinh(2u)]}$$

This analytical model allows a quick estimation of the effect of material properties, geometries and loads, without the need for computational modeling.

1.5 Chapter summary

Interest in the drop impact robustness of electronics is motivated by 1) the widespread use of mobile devices; 2) the weakness of lead-free solder joints under high strain rates; 3) the increased fragility of area array joints as a result of miniaturization; 4) deficiencies in existing test methods for assessing drop impact robustness; and 5) a lack of proven methodologies for predicting failure under drop impact. The research gaps introduced in Section 1.2 have been identified based on the literature review undertaken. In summary, there is a lack of both qualitative and quantitative information on impact-induced fatigue failure of solder joints in portable electronic devices. This deficiency is partly due to the use of test methods which do not reflect the loading conditions experienced during drop impacts of actual devices. Also, existing test methods do not have the capability of characterizing fatigue failure for the wide range of parameters that may be encountered in a device drop. A lack of fatigue data also limits the development of a practical life prediction models for solder joints. Several life prediction methodologies for solder joints subjected to complex load histories have been proposed over the years. These methodologies are typically based on the simple but practical use of S-N curves for fatigue characterization and the Palmgren-Miner Rule for cumulative damage estimation. However, none of these methodologies have been validated and shown to work for the variable load histories generated by drop impact.

Chapter 2

Crack Propagation in Solder Joints under Dynamic PCB bending

Chapter 1 has highlighted the generation of significant PCB strains when a mobile device is dropped, and that dynamic PCB bending is the dominant cause of solder joint failure in board-level drop tests. This chapter investigates the evolution of damage in a solder joint during each cycle of dynamic PCB bending, observed through in-situ monitoring of the crack growth in a solder joint [44].

2.1 Introduction: Damage evolution in solder joints

Previous studies which track the evolution of fatigue damage in solder joints have focused on damage evolution under thermal cycling fatigue and electromigration. These studies include: 1) observing general trends in crack propagation based on cross-sections of solder joints from thermal cycling fatigue tests [45-47]; 2) monitoring solder joint resistance changes associated with creep strain and damage [48-50]; and 3) monitoring resistance changes caused by electromigration damage, void formation and crack growth [51]. Because impact-induced fatigue is a very different phenomenon, involving much higher strain rates and different failure drivers, it is essential to also understand damage evolution under impact-induced fatigue. The experiments in this chapter provide a qualitative understanding of the link between impact of a portable electronic device, resulting PCB strain induced and failure of solder joints.

2.2 Experimental technique

Test vehicle

The test vehicle shown in Fig. 2.1(a) has both the board and component made from the same FR-4 PCB panel. Circuit board assembly is performed by a reflow process which attaches 0.4 mm solder balls to the component, followed by a second reflow to attach the bumped component to the board. With reference to the schematic diagram in Fig. 2.1(b), the solder joint height is approximately 300 μm, and the designed pad diameter (solder resist opening) is 300 μm. The PCB panel is 0.8 mm thick and the copper pad is 50 μm thick.

Electrical resistance measurement

Figure 2.1(c) shows the solder pad layout. The layout is designed for the monitoring of four individual joints located at the component corners on the test vehicle. These corner joints are offset towards the outer edges of the component by one joint pitch. Because board bending generates the highest stresses in joints along the edges, the offset corner joints experience slightly higher loads than other joints in the array, and are the first to fail during testing. Random failures are therefore prevented in the joints that are not monitored. Appendix A provides further details on how the test vehicle was designed to ensure independent results from the four joints monitored.

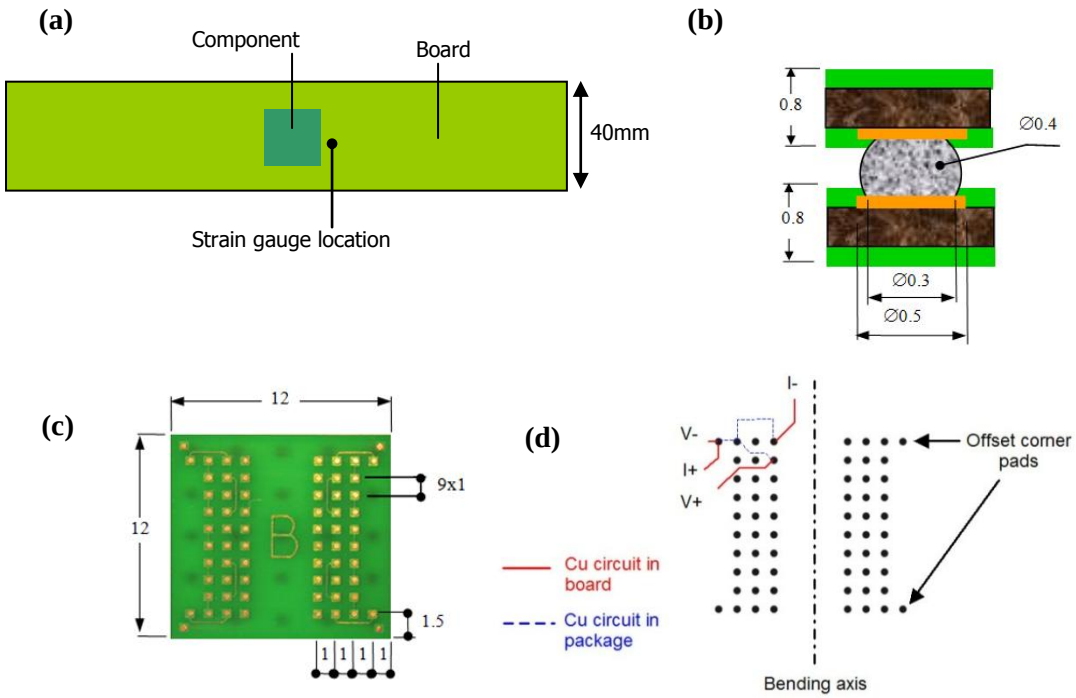


Figure 2.1: Test vehicle: (a) Schematic diagram of test vehicle; (b) Solder joint dimensions; (c) Solder joint pad layout; (d) Cu trace routings on board and component for four-point measurements.

Each corner joint has a separate circuit for monitoring resistance change. Resistance is measured using a four-wire (Kelvin connection) technique which eliminates lead resistances from the measurement. A schematic diagram of a corner joint circuit is shown in Fig. 2.1(d). A source current of 200mA is passed through each corner circuit through a pair of current-supplying leads/traces, and the voltage drop across the corner joint is measured by a pair of voltage sensing leads/traces which terminate adjacent to the corner solder joint. As negligible current flows through the voltage sensing leads, the resistance of the voltage sensing leads is eliminated from the measurement. This trace layout thus allows the measurement of resistance changes due to damage in a single joint. Tracking the resistance change in a single solder joint is advantageous, because it ensures that the measured resistance changes are caused only by damage evolution in that particular joint, thus aiding in correlating damage evolution to failure modes. The

absolute voltage measured is the potential drop across the solder joint and a short length of the copper traces. The minimum detectable resistance change is approximately 20 μΩ, which corresponds to the measurement noise floor. A 200 mA current level was selected as a compromise between minimizing Joule heating in the Cu traces and allowing an adequate voltage level for sensitive measurements. Before the start of mechanical testing, the current is applied for several minutes to stabilize temperature drifts and resistance fluctuations caused by Joule heating of the copper traces. Drop tests or dynamic bending tests are then performed, during which an oscilloscope tracks changes in the voltage drop across the joint due to damage in the solder joint. The tests continue until the occurrence of an electrical open, which indicates that a full crack has broken the electrical circuit. The graph in Figure 2.2 shows an example of the voltage difference measured across a solder joint during sequential drop/shock tests. Each drop raises the voltage potential difference. The experimental technique is therefore sensitive enough to resolve tiny voltage (resistance) increases due to solder joint damage arising from each drop. Further details on the experimental technique and instrumentation specifications are given in Appendix B.

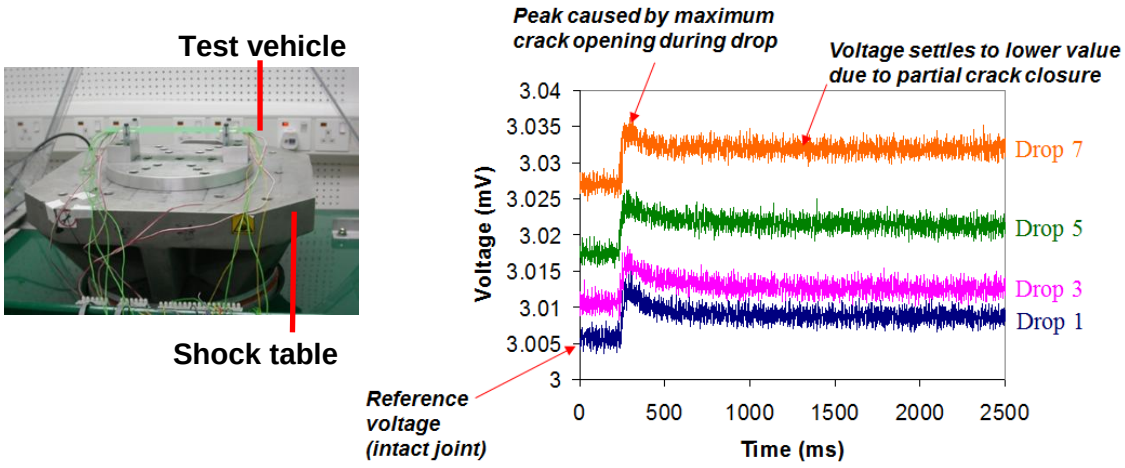


Figure 2.2: Voltage measurement across a solder joint over several drops, where damage to the solder joint increases resistance and therefore the measured voltage.

Relationship between crack area and electrical resistance

To obtain a relationship between the electrical resistance measurements and physical crack size, finite element modeling of electrical connectivity in cracked joints was undertaken. The cracks were modeled to have similar shapes as those in typical partial cracks observed in dye-and-pry tests. An explanation of the dye-and-pry method is given in Appendix B. The dyed fracture surfaces of Fig. 2.3(a) shows various stages of crack development caused by dynamic PCB bending. Figure 2.3(b) shows a solder joint finite element model with a crack along the board pad, modeled using ABAQUS v6.8. The electrical FE model consists of a solder ball and copper pads at the top and bottom of the solder ball. Intermetallic compound (IMC) layers are not modeled and the solder ball and copper pads are assumed to have homogenous isotropic material properties. The material properties are listed in Table 2.1. The coupled thermal-electrical analysis procedure in ABAQUS is used for simulation of steady-state current conduction. Voltage and current boundary conditions of the electrical FEA model are as indicated in Fig. 2.3(a). The crack is assumed to propagate along a horizontal plane at the interface between the copper pad and solder ball. The presence of a crack increases the voltage potential drop across the circuit; this can be seen in the contour plot of voltage potential in Fig. 2.3(c), where there is a high voltage potential gradient at the constriction caused by the crack. While the full experimental circuit may be modeled as shown in Fig. 2.4, it is sufficient to model only a single joint with its pads if the voltage potential change is limited to the vicinity of the crack within the joint. The ABAQUS mesh element DC3D10E (10-node quadratic coupled thermal-electric tetrahedron) is used in the entire model. The element size is 20 μm, which for a solder ball size of 0.4 mm results in approximately 50000 elements. This

mesh density is sufficient to ensure convergence of the potential drop taken across V+ and V-. As the crack area increases, the resistance of the solder joint increases exponentially as shown in Fig. 2.5, which is a plot of electrical resistance with crack area, for the case of a single crack adjacent to the board pad.

Table 2.1: Parameters used for steady state current conduction model.

Parameter	**Value**
Copper electrical conductivity	6.0 x 10^7 S/m
Solder electrical conductivity	7.2 x 10^6 S/m
Copper layer thickness	50 μm
Copper trace width	60 μm

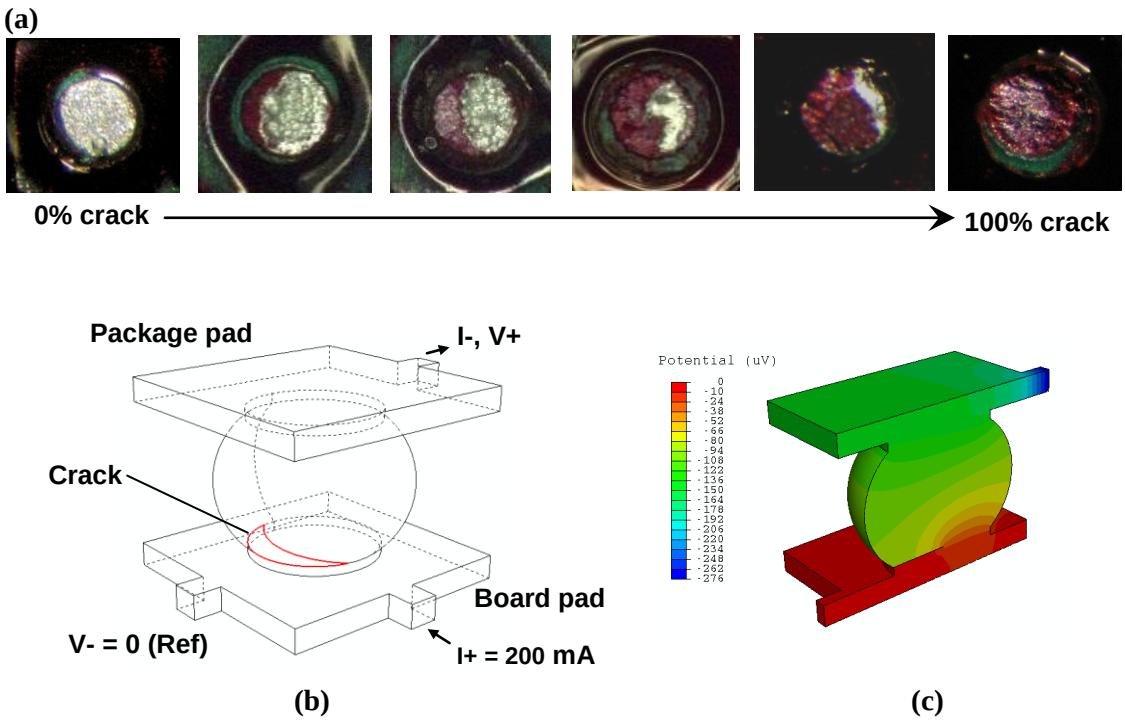


Figure 2.3: Modeling of cracked joints: (a) Dye-and-pry results showing progression of crack area and shape. (b) Model with crack. (c) Localized potential drop near crack.

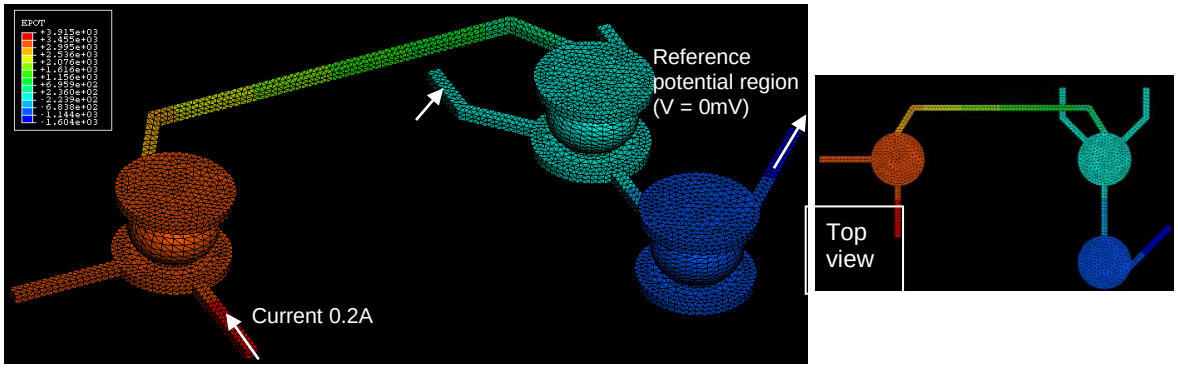


Figure 2.4: Electrical FEA plot of voltage potential across full solder joint circuit.

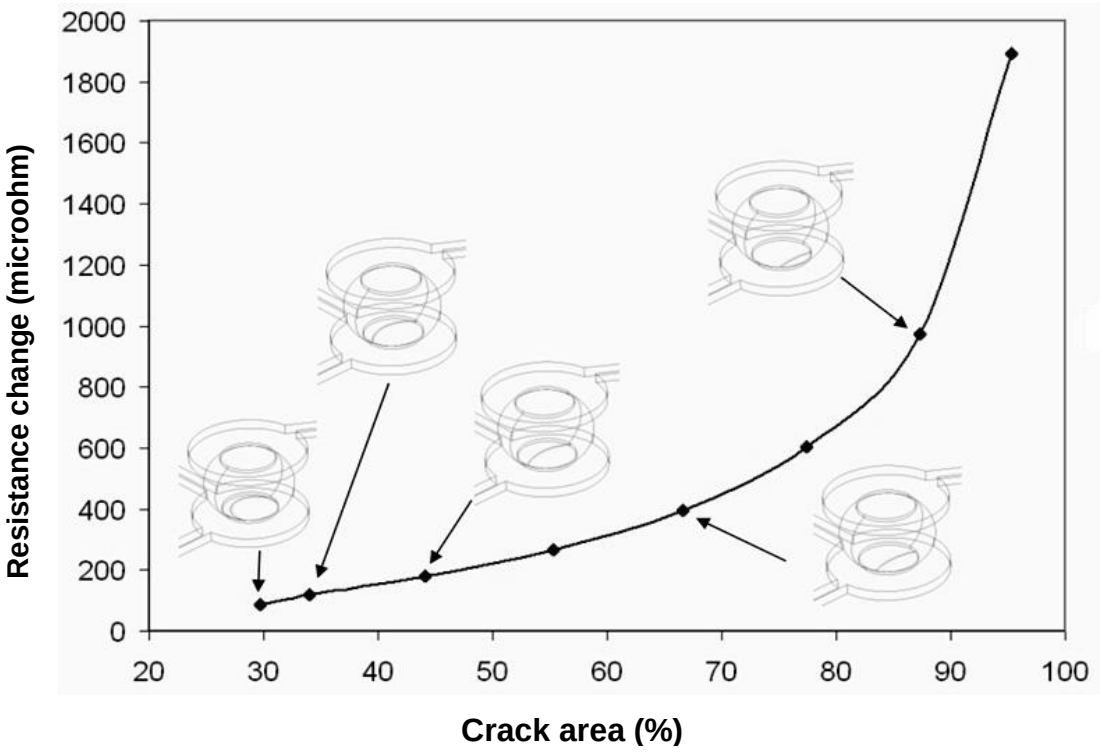


Figure 2.5: Variation of resistance change with crack area, obtained from FEA models with different crack sizes.

Validation of the model was performed by comparing experimentally-measured resistance changes with predicted values, for given crack areas. Appendix B (Table B.1) shows results of the validation study. The difference between the predicted and measured resistance in several cases exceeds 20%. This is attributed to manufacturing variations in the dimensions of the solder joint, pads and copper plating, as well as differences between the actual crack shape and the modeled

crack front. Because of these variations, the crack monitoring experiments described in this chapter should be viewed primarily as a study of patterns or trends in crack propagation.

High-speed dynamic bend tests

To study the effects of dynamic PCB bending on solder joint failure, it is essential to be able to reproduce in a controllable manner, the high bending strain amplitudes and frequencies observed in the drop impact of a portable electronic device. Cyclic four-point bending of circuit board samples was performed using the tester shown schematically in Fig. 2.6(a), which was specially designed to generate sinusoidal bending pulses at high frequencies and amplitudes that are associated with drop impact. The test vehicle is loaded in a four-point bending configuration, with an outer span of 60 mm and an inner span of 35 mm. The inner span is defined by two pairs of cylindrical rods; the upper rods are in contact with a loading anvil connected through a lever to a motorized rotary cam that imposes sinusoidal vertical motion, thus generating cyclic bending of the board. A bending strain pulse, measured by strain gages located on the board adjacent to the chip package, is shown in Fig. 2.6(b). Further details on the high-speed bend tester are in Appendix C.

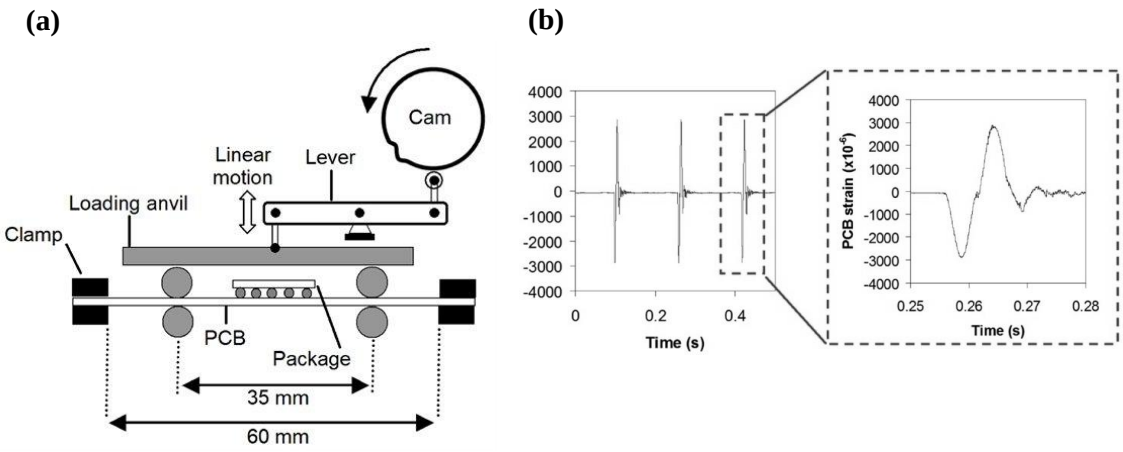


Figure 2.6: High speed bend tester: (a) Schematic diagram of tester; (b) Single sinusoidal pulse from bend tester.

2.3 Crack propagation characteristics in solder joints

The crack propagation results for joints made from three types of solder ball and pad material combinations (or material systems), each resulting in distinctive failure modes, are discussed in this section. The material systems used were:

1) Sn-37Pb solder on bare Cu pad: Solder joints made from this well-understood eutectic tin-lead (Sn-Pb) solder have consistently long fatigue lives.
2) Sn-1Ag-0.1Cu on bare Cu pad: Solder joints made from this new lead-free solder (SAC101) display good performance under drop impact, but exhibit a wider spread in fatigue life than eutectic Sn-Pb solder joints.
3) Sn-3Ag-0.5Cu on Cu pad with Ni-Au finish: Sn-3Ag-0.5Cu (SAC305) solder joints have excellent thermal cycling fatigue performance, but are known for their extremely poor performance under drop impact, especially if soldered onto copper pads with Ni-Au finish.

To bring these solder joints to failure, high speed cyclic bend tests were performed to simulate drop impact loading conditions. A sinusoidal bending waveform with a frequency of 100 Hz, a strain amplitude of 1800 microstrains and a strain ratio R = -1 was used for this study.

Figure 2.7(a) shows the crack growth progression in the eutectic Sn-Pb solder joint over its entire fatigue life. When the crack progression is observed over several bending cycles – as shown in the magnified view of Fig. 2.7(b) – a distinct pattern of peaks and troughs can be seen, and this reflects the sinusoidal bending pulses applied to the test vehicle. Positive bending strains cause the crack to advance, as indicated by the small peaks in the waveform. Negative bending strains cause the fractured crack surfaces to come back into contact with one another, resulting in a momentary crack closure, a drop in electrical resistance, and a sharp trough in the waveform.

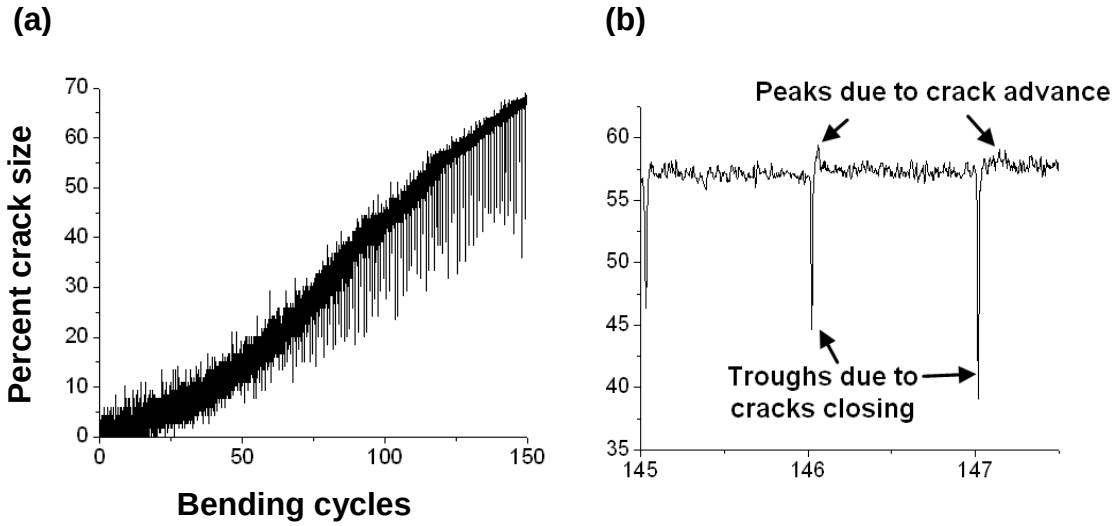


Figure 2.7: Crack monitoring results for eutectic Sn-Pb on a bare copper pad:
(a) Plot of crack size against number of bending cycles.
(b) Magnified view of results for several cycles.

In Fig. 2.8(a), the peaks and troughs have been filtered out to show a clearer view of the crack growth trend. Figure 2.8(b) shows a scanning electron micrograph of a cross-section of the failed joint, indicating that the crack propagates entirely within the bulk solder material. The arrows in Fig. 2.8(b) indicate the direction of crack propagation. Cracks begin at the pad edges due to the stress concentration and high material strain rates at these locations.

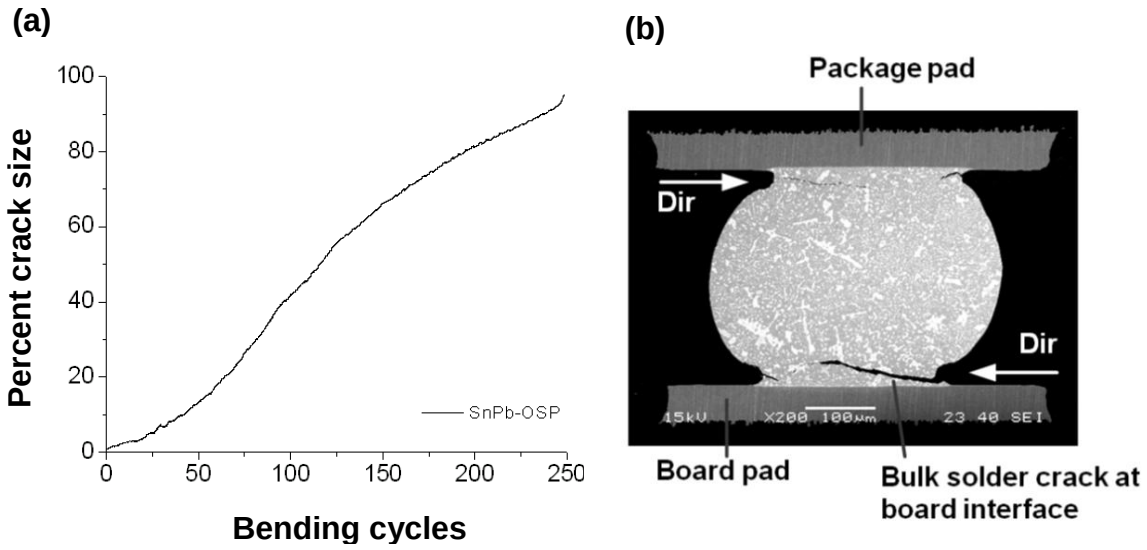


Figure 2.8: (a) Crack size vs bending cycles for eutectic SnPb on a bare copper pad. (b) Cross-section showing corresponding failure mode.

It is observed that fatigue cracks start to grow almost immediately from the first bending cycle, without a discernible crack initiation phase. Initial crack growth occurs at an increasing crack growth rate, as indicated by the rising gradient of the curve. After a certain point (at approximately 100 bending cycles), the crack growth rate starts to decrease; this is indicated by a drop in the gradient of the curve. As cyclic bending continues, the crack grows until there is too little solder left to maintain a mechanical connection, resulting in a final rapid rate of fracture propagation, as indicated by the sharp upturn at the end of the curve. This pattern is

hypothesized to be due to two opposing effects on the crack driving force: 1) an increase in crack size causes an increase in the crack driving force; and 2) an increase in compliance of the joint resulting from the presence of the crack reduces the crack driving force. When the crack is small, the former effect dominates but as the crack grows, the latter becomes more dominant. This "S-shaped" trend is observed to be typical of cracks occurring in bulk solder.

Figures 2.9(a) and 2.9(b) show the crack growth and failure mode for the SAC101 joint on bare copper. The joint exhibits a mixed failure mode, whereby the crack starts in the bulk solder, propagates into the IMC region for a short distance, then returns to the bulk solder. The corresponding crack growth curve reflects this behavior, where the marked section of the curve with a steeper gradient is attributed to rapid crack growth along the IMC layers.

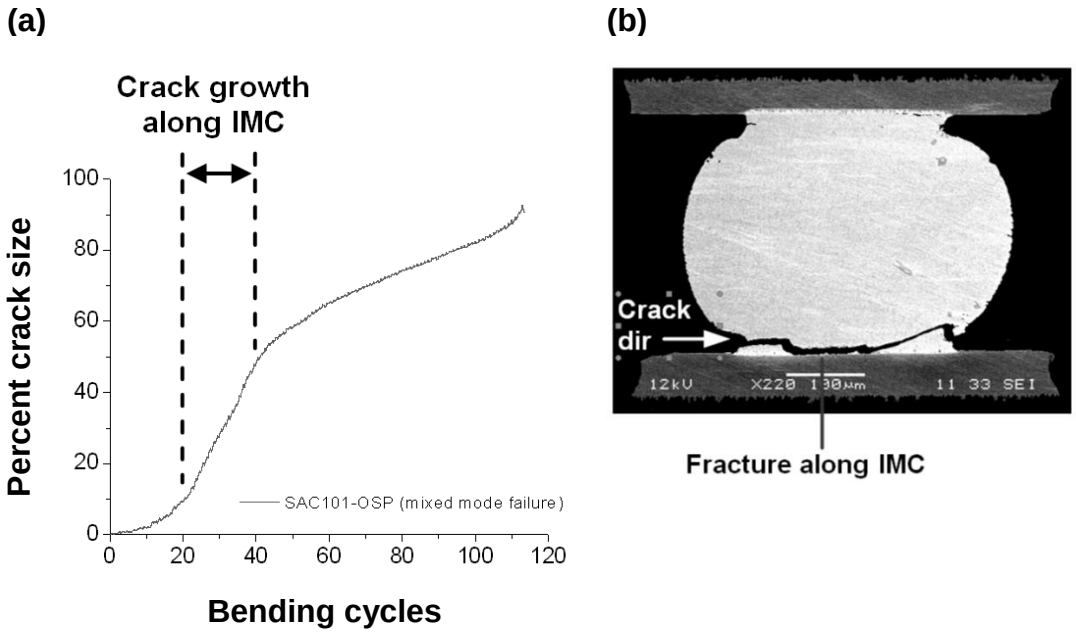


Figure 2.9: (a) Crack size vs bending cycles for SAC101 solder on bare copper pad. (b) Cross-section showing corresponding failure mode.

Figures 2.10(a) and 2.10(b) show the crack growth and failure mode for an SAC305 joint on Ni-Au finished Cu pads. There is a narrow crescent of bulk solder material at the right edge of the pad where the crack initiated. The remainder of the pad exhibits failure within the IMC layers. Crack growth is initially gradual, until a point is reached, when there is a sudden catastrophic failure of the joint, indicated by the vertical portion of the crack growth curve. Much of the fatigue life is spent propagating a crack across a small area of the pad, and to advance the crack in the ductile and tough bulk solder material. In contrast, crack growth across the wide IMC region occurs within only one or two bending load cycles.

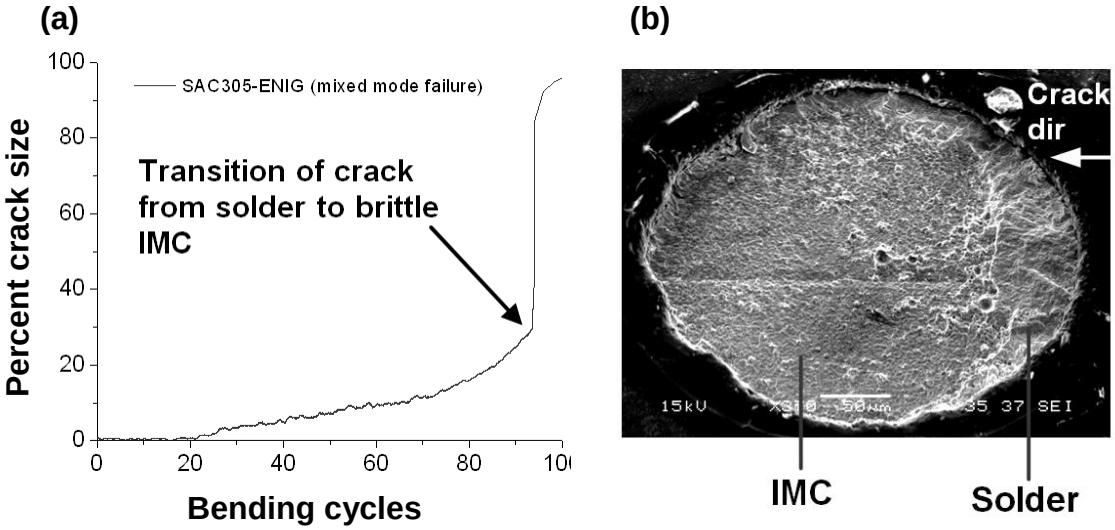


Figure 2.10: (a) Crack size vs bending cycle signal for SAC305 on Ni-Au finished pad. (b) Fractograph of failed pad showing corresponding failure mode.

The observations described above regarding IMC failure for lead-free solder joints demonstrate a critical issue encountered when manufacturers switched from tin-lead solder to lead-free solders. Lead-free solder joints were observed to be more susceptible to brittle IMC failure than Sn-Pb joints, especially under the high loading rates associated with drop impacts. In general, high loading rates have two effects: 1) they raise the stress levels in the solder, thus causing them to exceed the

strength of the brittle IMC layers; and 2) they promote cracks in the bulk solder material, whereas at lower strain rates, the material would stretch and deform. Once a crack has formed in the solder joint, failure may be rapid or gradual, depending on the path taken by the crack along the solder pads.

2.4 Chapter Summary

This study involves monitoring impact-induced fatigue crack growth in solder joints via in-situ measurement of the electrical resistance of a single solder joint during dynamic PCB bending. The fatigue crack initiation period is practically negligible, as cracks develop in a solder joint within the first few loading cycles. For cracks that run completely within the bulk solder, crack growth is steadily progressive up to the point of final fracture. For a mixed mode fatigue crack growth, acceleration in the crack growth is observed when the crack transitions from propagating within the bulk solder to propagating along IMC layers. The crack monitoring technique used in this study confirms a direct link between damage progression and failure modes, whereas previously, such patterns could only be inferred.

Chapter 3

System-level Investigation of Solder Joint Failure

The previous chapter has discussed how fatigue cracks grow in solder joints under stresses that develop as a result of impact-induced dynamic PCB bending. This chapter investigates how these phenomena occur in a portable electronic device (mobile phone) when it is subjected to drop impact. This system-level investigation provides test conditions as close as possible to field conditions, and tracks the failure process of a solder joint in an electronic device over several drops.

3.1 Experimental technique

In order to track solder joint damage during drop impact of a mobile phone, the original PCB assembly of the mobile phone is replaced by an instrumented board assembly, designed for in-situ tracking of solder joint cracks during each drop.

The mobile phone (Nokia 3110c), with its original board and the instrumented board, is shown in Fig. 3.1. The edge profile of the instrumented board was machined to match the profile of the original board, thus allowing it to fit within the casing of the phone. The instrumented board assembly consists of an electronic component mounted via 0.4mm diameter solder joints onto a 0.8mm-thick PCB. The solder joint layout (Fig. 3.2) is identical to that used in the crack propagation study described in Chapter 2, with one corner solder joint electrically connected for high-sensitivity 4-point electrical resistance measurements. A strain gauge is mounted on the PCB, adjacent to the component but on the opposite side, so as to

record dynamic strains during drop impact. Two instrumented boards with different solder-pad material systems were used in this study: 1) SnPb solder balls on ENIG pad finish; and 2) SAC101 solder balls on Cu(OSP) pad finish.

The mobile phone was dropped from a height of 1 m, with the bottom of the phone impacting a rigid surface at an angle of 45°. Figure 3.3 shows high-speed camera images of the phone in the 45° drop orientation.

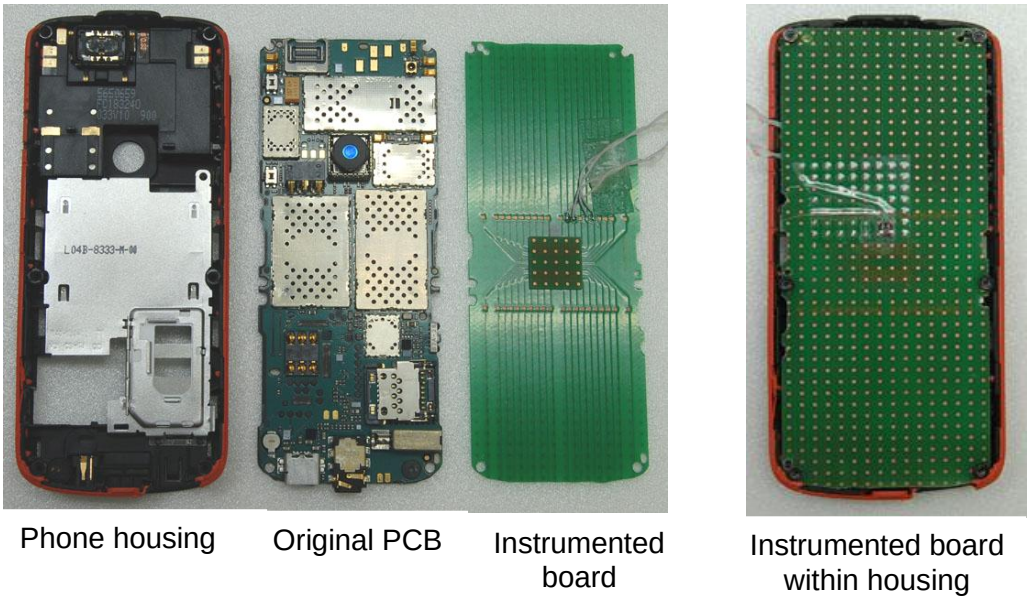


Figure 3.1: Mobile phone (Nokia 3110c) used for in-situ resistance measurements during product drop tests, with original PCB assembly and instrumented board shown.

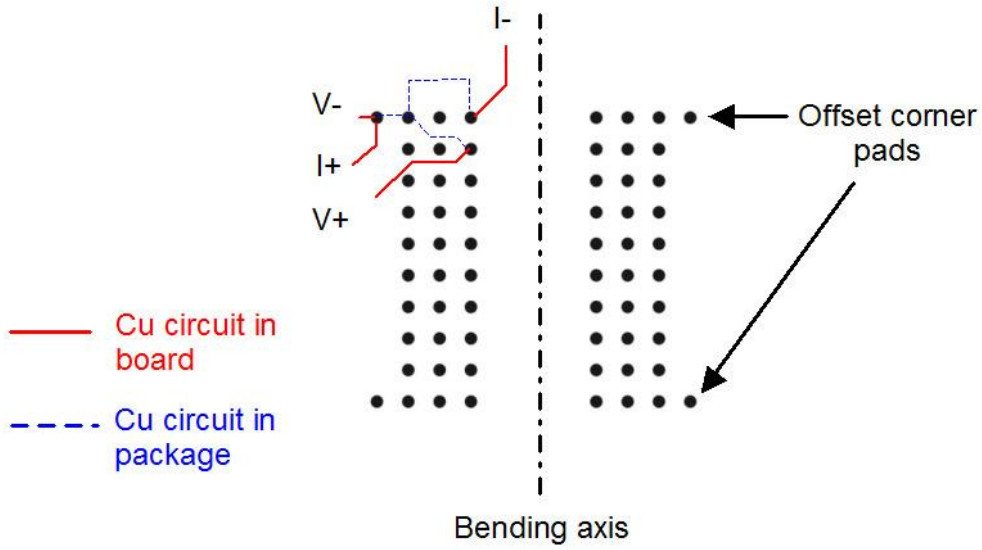


Figure 3.2: Solder joint layout for 4-point resistance measurement.

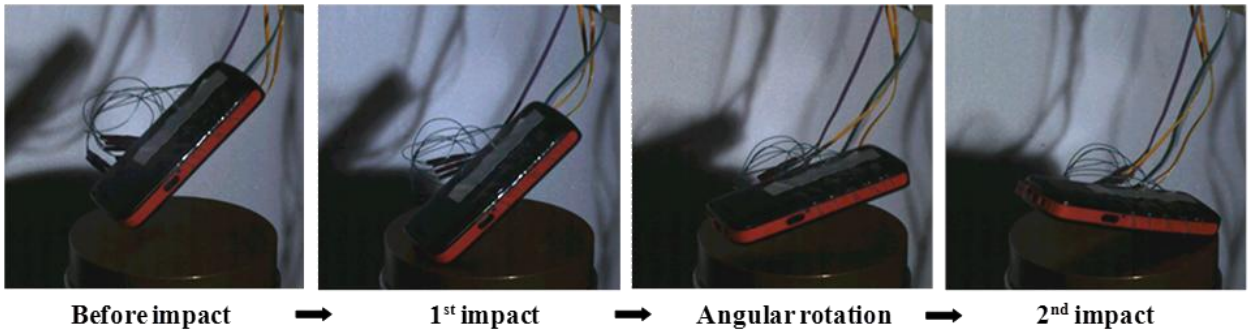


Figure 3.3: High-speed camera images of Nokia 3110c phone dropped at 45° orientation.

3.2 System-level Test Results for SnPb-ENIG joint

Figure 3.4 shows results in terms of the dynamic PCB strain (red curve), crack area (black curve) and impact force (blue curve) during the first drop test of the mobile phone, which had an instrumented SnPb-ENIG board incorporated. The key events occurring over a 20 millisecond period are numbered and labeled.

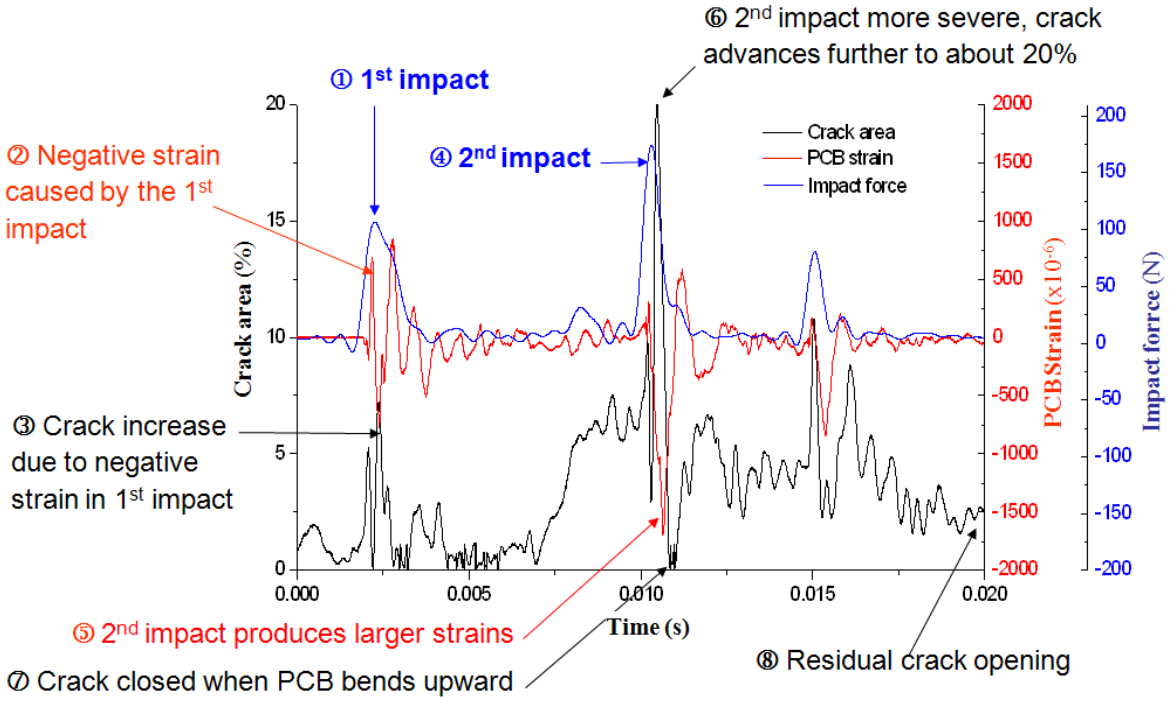


Figure 3.4: PCB strain, crack area (from resistance measurements) and impact force during first drop of mobile phone sample.

Within this short time span, there were three impacts of the mobile phone against the impact surface; indicated by three peaks in the impact force curve. Matching the first load cell pulse to the instant of the first impact observed in the high speed video reveals that the multiple impacts are caused by clattering of the phone. The first two impacts can be seen in the high-speed camera images of Fig. 3.3, and correspond to the first two peaks in the impact force curve. The first and second peaks are labeled ① and ② respectively in Fig. 3.4.

Each impact induces dynamic bending in the PCB; this is measured by the strain gauge mounted on the PCB. The dynamic strain response (red curve) indicates that bending of the PCB occurs soon after the commencement of each impact against the rigid surface. The second impact is by far the most severe, generating a strain peak ⑤ of approximately 1500 microstrains at a frequency of 800 Hz. It should be

noted that because the strain gauge is mounted on the side of the PCB opposite to that which the component is attached, compressive or negative strains indicate that the PCB bending is "stretching" the perimeter solder joints. The mechanics are illustrated in Fig. 3.5.

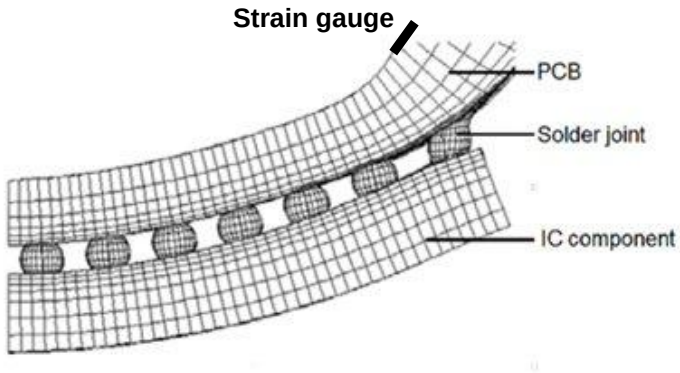


Figure 3.5: Strain gauge on side of PCB opposite to that on which component is attached, measures compressive strains when perimeter joints are stretched.

The dynamic PCB bending in turn causes damage and crack growth in the solder joint being monitored. The crack area (black curve) is inferred from electrical resistance measurements, and indicates that the first impact induces a crack with an area roughly 7% (indicated by ③) of the total pad area. Note that the crack area "decreases" with a decrease in the dynamic bending strain because in the absence of bending, the crack surfaces come back into contact with each other, thus reducing the measured electrical resistance. However, the crack surfaces can subsequently be separated by flexural strains that are much smaller than that which initiated the crack. The severe second impact causes the crack area to increase to approximately 20%, as indicated by ⑥. Also, flexure of the PCB in the opposite direction can result in complete crack closure, as indicated by ⑦. Owing to wear or compression of the crack surfaces through multiple flexural oscillations, a residual crack opening ⑧ remains after the 3rd impact, even when bending ceases.

Table 3.1 summarizes the sequence of events occurring during the particular drop impact described above.

Table 3.1: Sequence of events during drop impact test.

Label	Event
①	First impact contact of mobile phone with load cell surface.
②	PCB strain induced as a result of first impact.
③	Solder joint damage (crack formation) arising from PCB strain induced during first impact.
④	Second impact of phone due to clattering.
⑤	Large PCB strain induced as a result of second impact.
⑥	Crack grows due to strains induced by second impact.
⑦	Crack closes temporarily during reverse PCB bending.
⑧	Crack remains open even after dynamic PCB bending has damped off.

The preceding analysis of Fig. 3.4 points to a direct link between PCB bending and solder joint damage during the drop impact of a mobile phone. A significant crack in the solder joint is initiated by the first drop test, owing to the significant bending strains generated. The ultimate life of the solder joint, or the number of drop impacts it can sustain, depends on the damage accumulated over multiple drops. This cumulative damage is investigated by tracking the crack growth in the solder joint over multiple drops, until complete failure of the joint, indicated by an open circuit associated with complete separation of the crack surfaces.

Figure 3.6 shows the crack area and PCB strain responses monitored over 11 drop tests of the mobile phone. The signals for each drop event represent a window of 20 milliseconds (as in Fig. 3.4), and are plotted sequentially on the same graph as if there were no experimental setup time separating the drops. A unique colour is used to differentiate the signals of each drop impact from others. The graphs provide an overall view of damage progression over the life of the solder joint.

In the overall view of Fig. 3.6, the measurements for Drop 1 are identical to those in Fig. 3.4, but compressed horizontally because of the difference in the scale of the time axis. Nevertheless, several important features are still evident, namely: 1) the crack area grows to 20% during the significant bending (see strain signal) of the 2nd impact, as indicated by the dominant peak in the crack area curve; and 2) there is a residual crack opening at the end of the impact event. From Drop 2 to Drop 9, there is very little crack growth beyond that generated in Drop 1. Drop 6 appears to advance the crack slightly beyond 20%, owing to the higher peak strains that exceed 2000 microstrains in this particular drop.

Therefore, from Drop 2 to Drop 9, the initial crack that formed in Drop 1 has either been arrested or it experienced a much lower crack driving force. However, in Drop 10 there is a sudden jump in the crack growth. In the subsequent drop (Drop 11), the joint fails completely by separation from the solder pad. The reason for this catastrophic failure is next examined through a failure analysis of the crack surface.

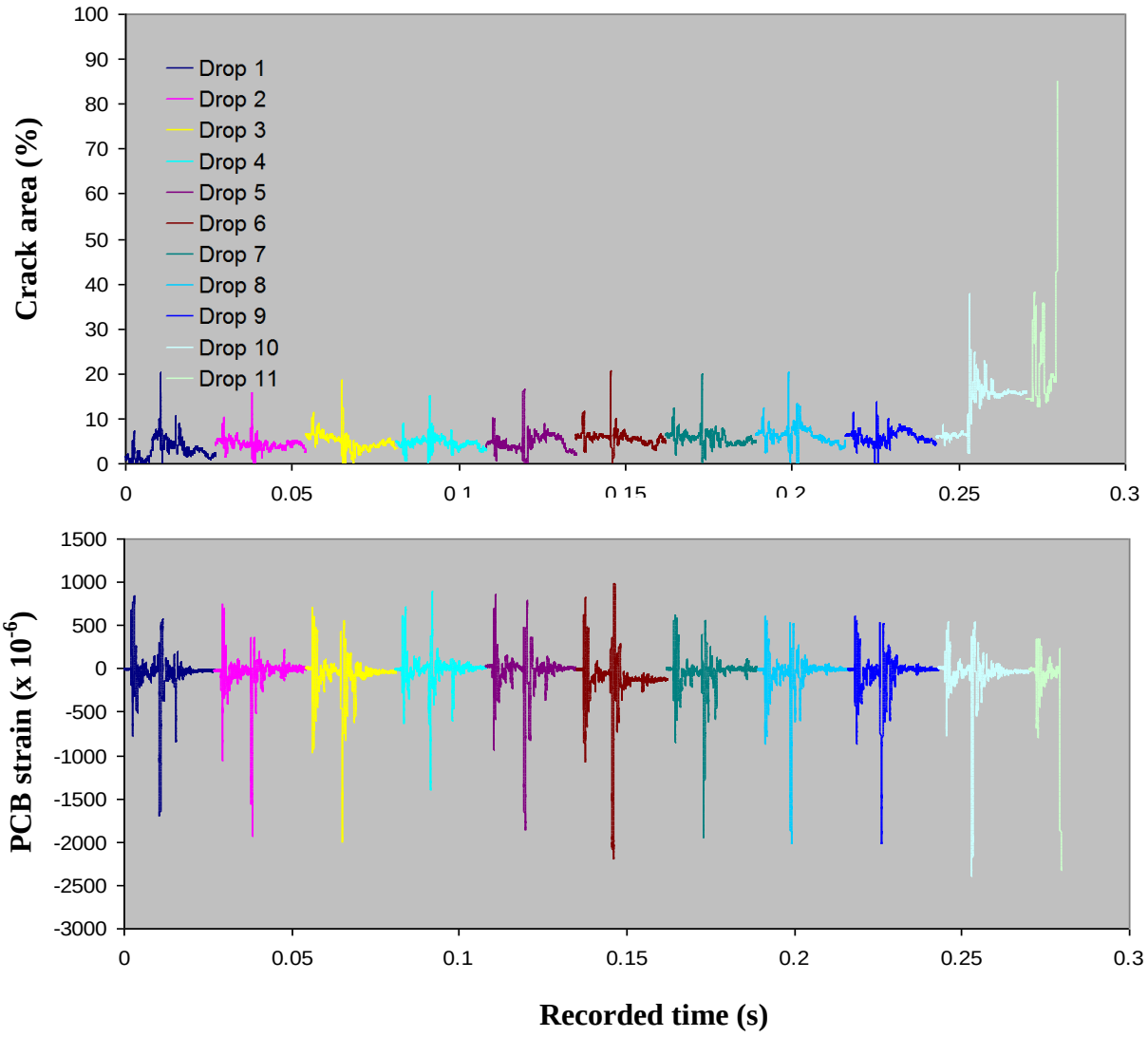


Figure 3.6: Crack area and PCB strain for sequential drops of mobile phone (SnPb-ENIG board)

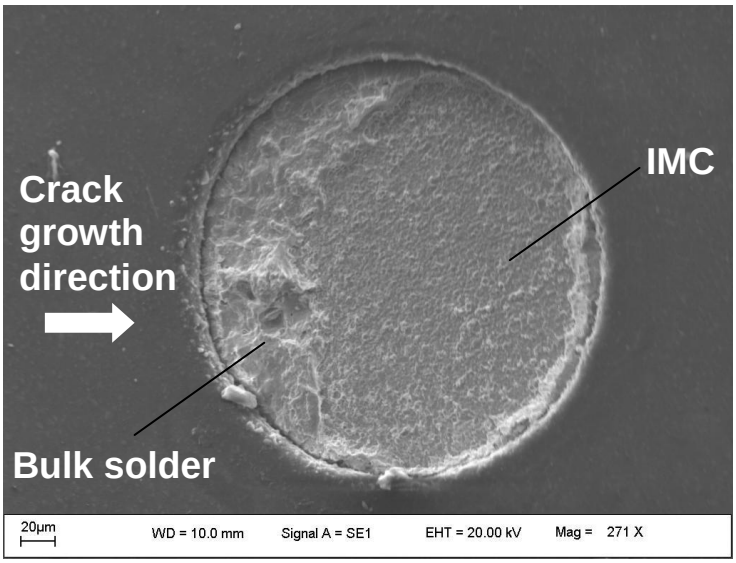


Figure 3.7: SEM fractograph of pad of monitored solder joint (SnPb-ENIG board).

Figure 3.7 shows a scanning electron microscrope (SEM) fractograph of the separated solder pad containing the crack surface. The crack growth is from left to right. There is a distinct bumpy crescent of material that is bulk solder on the left side of the pad, verified by SEM-EDS analysis. The remaining area of the pad on the right of the crescent is relatively smooth, and this is predominantly the brittle intermetallic compound (IMC) interface between bulk solder and copper pad. In Drops 1 to 9, the crack was likely confined within the crescent of ductile bulk solder material. However, in Drop 10 the crack path eventually entered the brittle IMC layers, where the crack propagated rapidly and unstably, aided by the high strain rates caused by dynamic loading.

The crack progression and failure for the SnPb-ENIG solder material system just analysed, has a complex nature. Much of the solder joint life – in terms of drops-to-failure – is expended propagating a tiny crack through a small area of bulk solder material. Once the crack front enters an area of weakness (brittle IMC) only a single drop is needed to propagate the crack through most of the pad area. Crack

growth in a solder-pad material system which yields a more consistent failure mode is next investigated.

3.3 System-level test results for SAC101-OSP joint

Figure 3.8 shows the damage progression in a system-level test using an SAC101-OSP material system. The drop test parameters are the same as the previously discussed SnPb-ENIG material system. In this case, 25 drops were needed to bring the solder joint to complete failure.

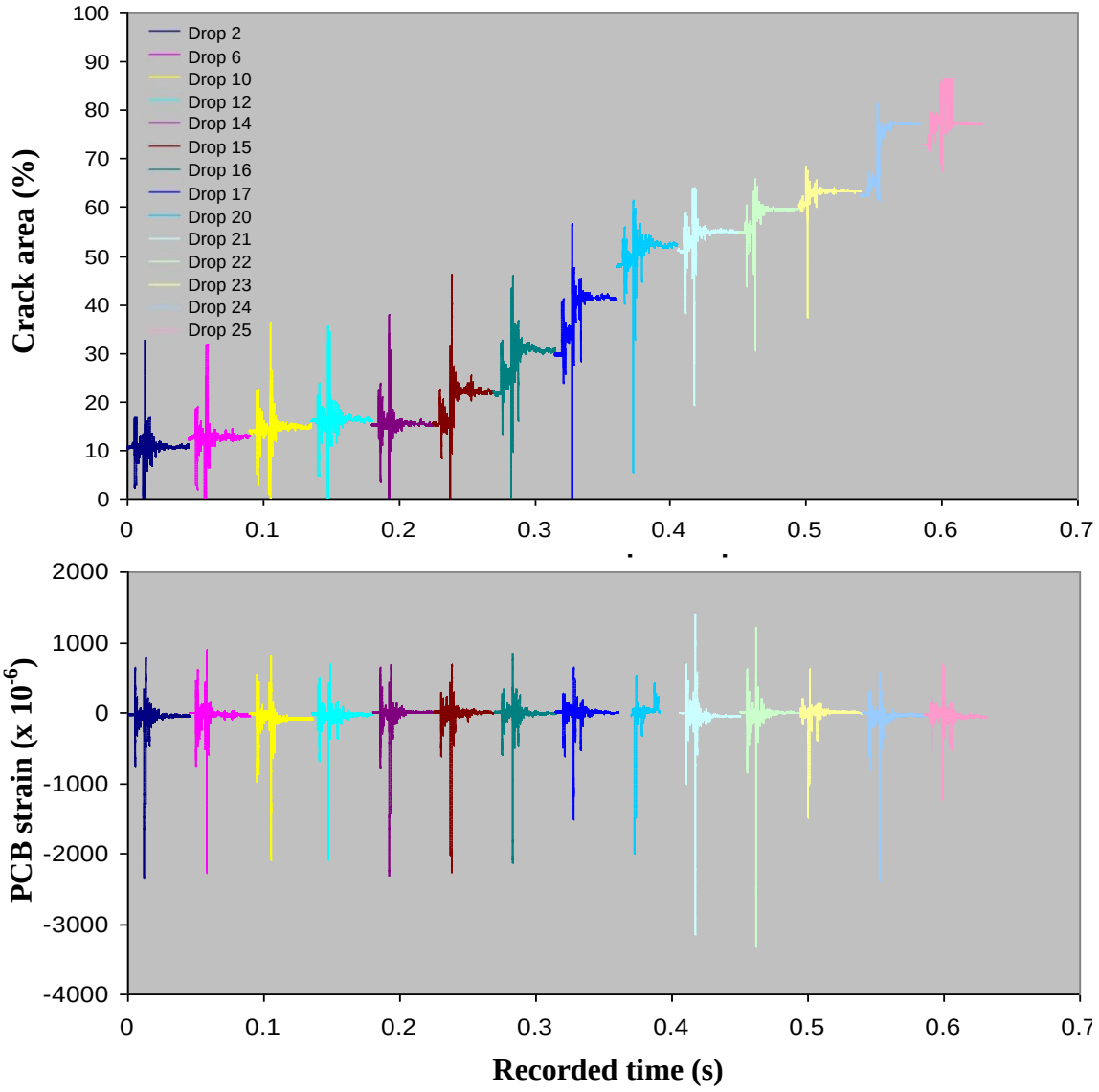


Figure 3.8: Crack area and PCB strain response over sequential drops of a mobile phone (SAC101-OSP board)

Crack growth from drops 1 to 14 is initially slow, as in the SnPb-ENIG case. However, after Drop 14, the crack grows significantly but stably with each subsequent drop impact. Interestingly, the much higher bending strains generated in Drops 21 and 22 do not cause an acceleration in the crack growth rate.

The SEM fractograph of the failed pad surface in Fig. 3.9 provides an explanation for the gradual crack growth in the SAC101-OSP material system. There is a far greater amount of bulk solder material remaining on the surface of the pad compared to the SnPb-ENIG pad of Fig. 3.7, indicating that the crack had to propagate through ductile bulk solder material throughout the entire damage process. While IMC failure surfaces are observed (labeled in Fig. 3.9), they are largely surrounded by regions of bulk solder material, which prevented unstable crack propagation.

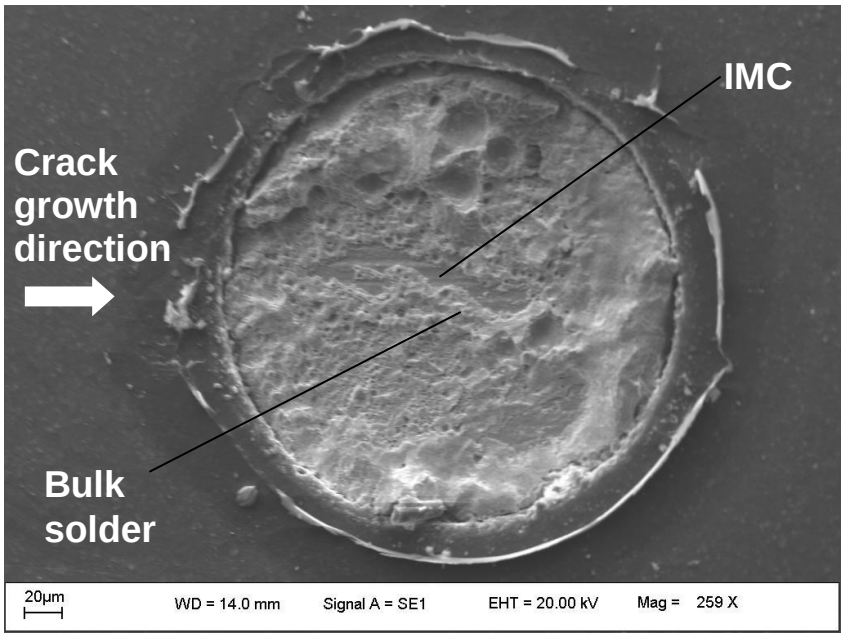


Figure 3.9: SEM fractograph of pad of monitored solder joint (SAC101-OSP board).

3.4 Chapter Summary

Drop impact experiments were performed on mobile phone samples with instrumented boards incorporated into them to enable in-situ tracking of solder joint damage during each drop impact. The results demonstrate how the impact force on the phone exterior excites dynamic flexural strains in the PCB, and how these strains in turn generate damage to the solder joints connecting the component and the PCB. These experiments yield an account of how cumulative damage occurs – from crack initiation to complete electrical failure – in the solder joint under realistic field conditions.

Two boards with different material systems were tested. For the SnPb-ENIG board, the solder joint exhibited mixed mode failure. Slow crack growth occurred in the bulk solder, followed by rapid unstable crack propagation along the brittle IMC interfaces due to the high strain rates generated during impact. The occurrence of brittle IMC failures is common in impact-induced fatigue, and rarely happens under conditions of thermal cycling fatigue or electromigration. For the SAC101-OSP board, crack growth was stable throughout the failure process, as crack growth occurred predominantly in ductile bulk solder material.

Chapter 4

Fatigue Characterisation of Solder Joints

Chapter 3 has described the complex load histories experienced by a mobile phone and its internal components during drop impact, and shown how different joint materials can exhibit widely varying failure modes and fatigue lives. To further understand the drop impact problem, this chapter investigates the effect of various parameters on the fatigue life of solder joints. These include material factors as well as load parameters that constitute the complex load histories.

4.1 Experimental approach

The goal of this fatigue characterization study is to provide data and information which can be used for developing failure models/methodologies for predicting solder joint failure under drop impact. In order to undertake a comprehensive characterization of solder joint fatigue, several parameters were identified for investigation. These are:

1) Solder material and pad finish combination (material system);
2) Magnitude of load (PCB strain amplitude);
3) Loading rate (PCB bending frequency);
4) Environment temperature;
5) The order in which variable loads are applied to the solder joint (load sequence).

This investigation consists of two main parts. The first (Sections 4.2 to 4.4) involves the use of the high-speed cyclic bend tester (HSCBT) to study the effects

of variations of individual parameters on fatigue failure of solder joints. Experimental fatigue data is condensed into fatigue S-N curves, which define the relationship between PCB strain and the number of cycles-to-failure. The second part of the study (Section 4.5) uses the S-N curves generated in Part 1, as well as crack growth monitoring, to determine the effects of complex load histories (sequencing) on fatigue failure.

Test samples (described in Appendix A) are brought to failure using the HSCBT (described in Chapter 2 and Appendix C), which facilitates dynamic bend tests that accommodate prescription of load amplitude, frequency and temperature parameters.

Table 4.1 shows the test matrix used. To study the influence of material systems, a range of solder materials were tested, using a common PCB bending strain amplitude and frequency. Eutectic SnPb is a well-established solder joint material used for several decades before the introduction of lead-free solder. SAC305, with its relatively high silver content (3%), is known to have good thermal cycling fatigue properties but poor robustness under shock due to the formation of Ag-Sn platelets, which form stress concentrations in the microstructure of solder joints. Conversely, SAC101 with its lower silver content (1%) forms joints which have robust performance under shock but poor performance under thermal cycling. SN100C is a low-silver eutectic solder which has Ni-dopants (0.05%) to control IMC growth. To examine the influence of amplitude/frequency and temperature, tests were performed on a few selected material systems but over a range of load amplitudes, in order to generate data for constructing S-N curves.

Table 4.1: Test matrix for fatigue characterization of solder joints.

	Study of aterial system influence	**Study of amplitude & frequency influence**	**Study of temperature influence**
Solder alloys	SN100C-0.6% Cu SN100C-0.8% Cu SAC305 Eutectic SnPb SAC101(Ni doped)	SAC101 SN100C (0.8% Cu)	SN100C (0.6% Cu)
Pad finish	Cu / OSP ENIG (Ni-Au finish)	Cu / OSP	Cu / OSP
PCB strain amplitude (microstrain)	2000 (Cu / OSP pad) 1200 (ENIG pad)	1000 to 3000	2000
Bending frequency (Hertz)	100	30 to 150 (SAC101 on OSP) 50 to 200 (SN100C on OSP)	100
Temperature ($^{\circ}$C)	22 (Room temp)	22 (Room temp)	0 ºC, Room temp
Number of samples	At least 8 and up to 32 solder joint samples for each test condition Exact numbers of samples used are indicated in Table D.1 of Appendix D		

4.2 Influence of material system

Comparison between high speed cyclic bend tests and board-level drop tests

Figure 4.1 shows HSCBT test results for various solder materials attached to copper pads with an organic solderability preservative (OSP) finish. The data is plotted in terms of cumulative percentage failure against number of bending cycles-to-failure. The plot provides an overview of the robustness of different solder materials relative to each other, as defined by the relative positions of their respective datasets along the cycles-to-failure axis. Board-level drop tests were also performed on these material systems to verify that the HSCBT tests are able to reproduce the load conditions and failure modes experienced in drop impact; the drop test results are shown in Fig. 4.2. The cumulative percentage failure plots for the two test methods show almost identical rankings of robustness of the various material systems, with SN100C and SAC305 joints being the most and least robust, respectively. An error analysis of the fatigue data from the HSCBT tests can be found in Appendix D. The SN100C samples exhibit excellent consistency in fatigue life, as indicated by the relatively low standard deviations of the SN100C datasets.

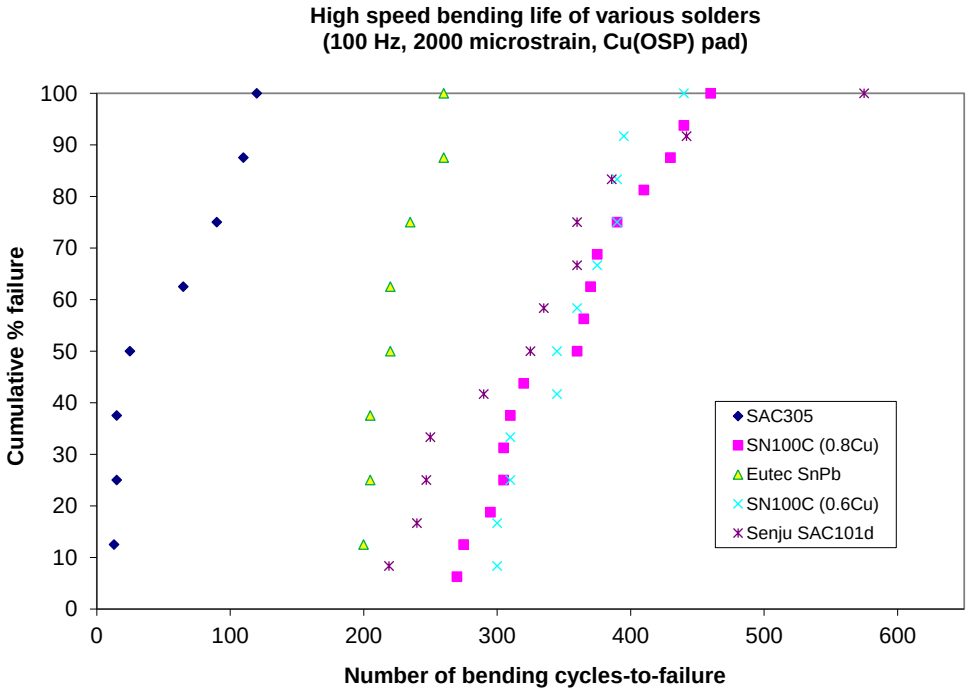


Figure 4.1: High speed bending fatigue life for various solders on bare copper pad.

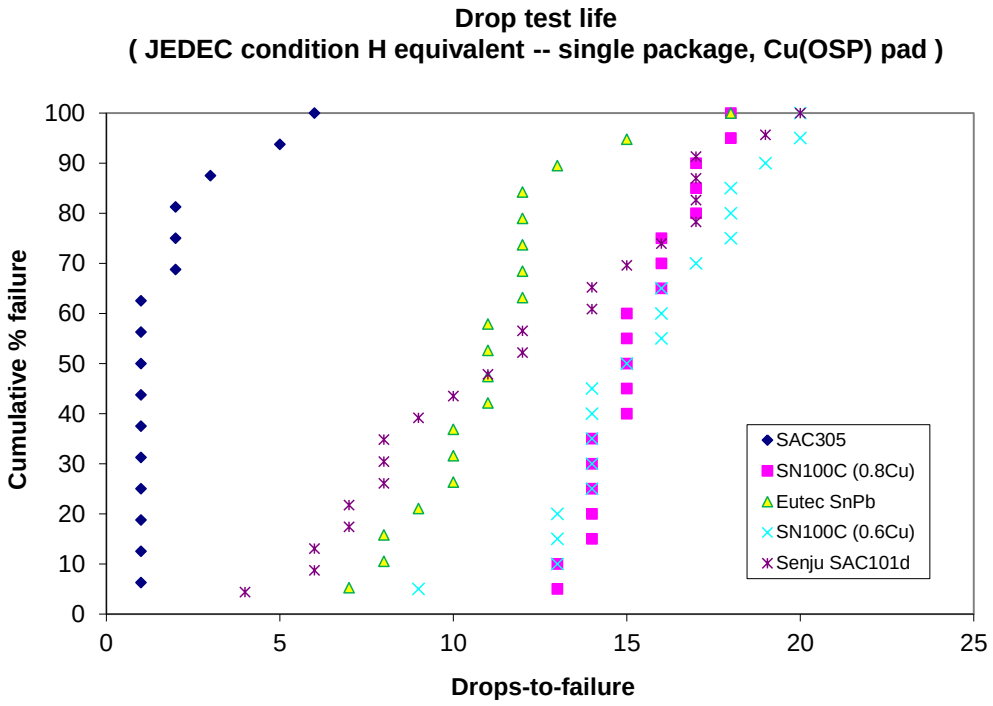


Figure 4.2: Drop impact life for various solders on bare copper pad.

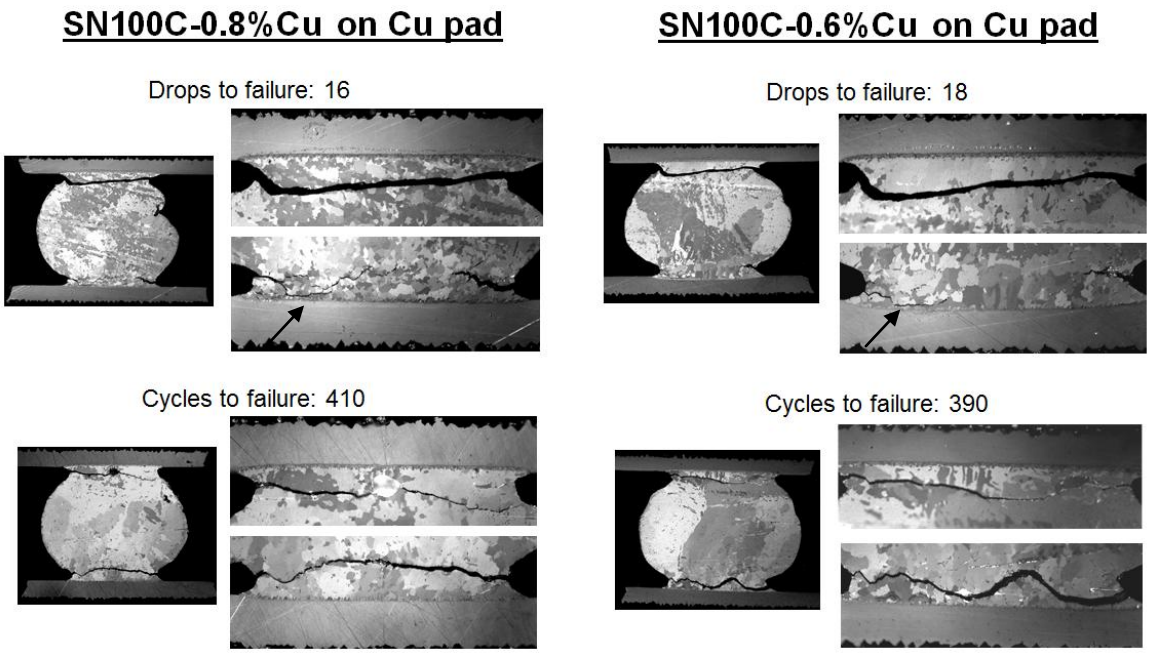


Figure 4.3: Comparison of failure modes for HSCBT and board level drop tests, for SN100C material systems on bare copper pads.

Figure 4.3 shows a comparison of failure modes for HSCBT and drop tests, for SN100C materials on bare copper (OSP) pads. The high speed bend test is able to reproduce the failure modes in drop impact, which are characterized by cracks running predominantly through the bulk solder material. Note that for drop impact failures, cracks are observed to propagate along the IMC layers for a short distance, as indicated by the arrows in Fig. 4.3.

Fatigue life and failure modes of various solder materials on bare copper pads

Comparing the performance of the various material systems in Fig. 4.1, it is observed that the data for the three most robust solder materials – SAC101d, SN100C (0.6% and 0.8%) – overlap each other in the high cycles-to-failure region; this indicates that the best joints formed using one solder are as robust as those formed using the other two solders. However, there are several SAC101d solder

joints that are significantly weaker than the best SN100C joints. Also, Sn-Pb joints are consistently less robust than joints formed by the top three materials, while the SAC305 joints are very fragile under dynamic PCB bending. To gain an insight into the reasons for the differences in robustness among the materials, failure analysis was performed. Figure 4.4 shows failure modes for the various solders on bare copper pads; the number of cycles-to-failure is stated for each joint shown.

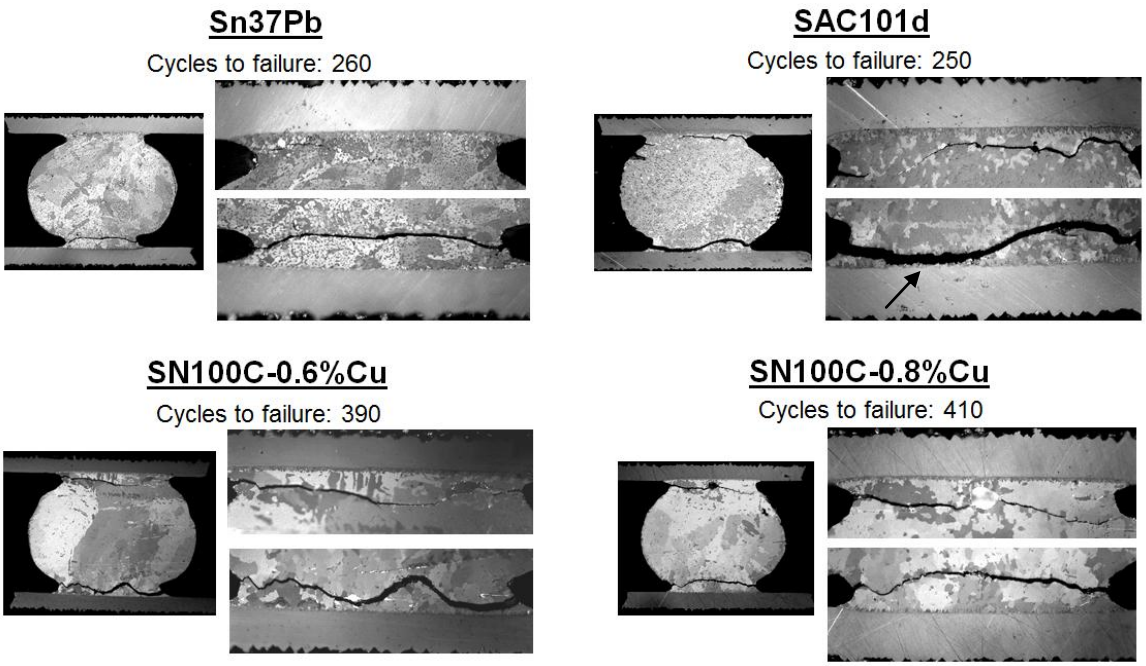


Figure 4.4: Failure modes under HSCBT for various solders on bare copper pads.

The reason for the lower robustness of Sn-Pb joints is hypothesized to be due to the straighter and therefore shorter crack path through the bulk solder material. In contrast, the crack paths through the SAC101d and SN100C solders tend to be more convoluted, likely due to microstructural features that force the crack to deviate from a straight path. The cross-section of the SAC101d solder sample corresponds to a data point indicating low cycles-to-failure (250 cycles). The

reason for the inferior robustness is that there is a significant length of crack in the IMC region, as indicated by the arrow in Fig. 4.4.

Fatigue life and failure modes of solder materials on Ni-Au finished pads

Figure 4.5 shows the robustness of various solders on Ni-Au finished (ENIG) copper pads subjected to HSCBT tests. There is significant data scatter owing to the susceptibility of ENIG-soldered joints to fail along the IMC layers. At the high end of the fatigue life range, the performance ranking of joints on ENIG is similar to that of joints on bare copper (OSP) pads (Fig. 4.1). However, at the lower end of the fatigue life range, the graphs converge, owing to the random nature of IMC failures. It should be noted that for this investigation of joints on ENIG pads, the HSCBT load amplitude was reduced to 1200 microstrains – compared to 1800 microstrains for bare Cu (OSP) pads – to prevent excessive IMC failures.

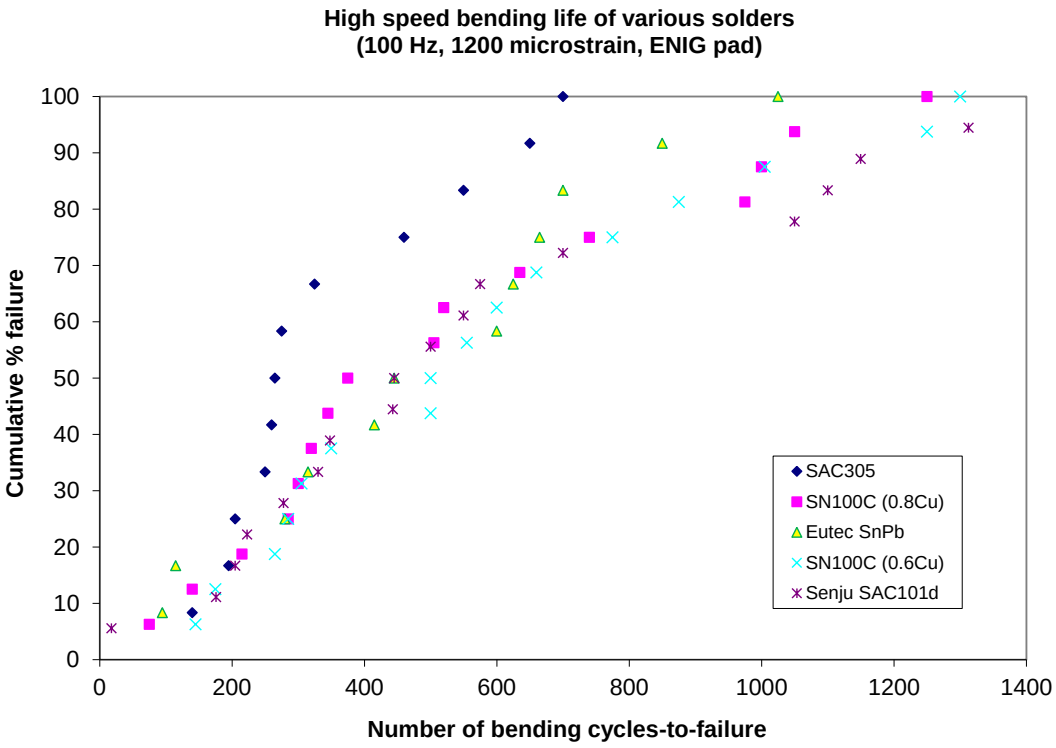


Figure 4.5: High speed bending life for various solders on ENIG pad.

Failure analysis was performed on samples which exhibited very different fatigue lives, for a given solder material. The failure analysis images in Fig. 4.6 show two examples each of robust and fragile joints – representing the extreme ends of the fatigue life range – for SN100C (0.6%Cu) solder material on ENIG. The difference between the fatigue lives at these two extremes is approximately fourfold. Low fatigue lives correspond to extensive cracking within the IMC region.

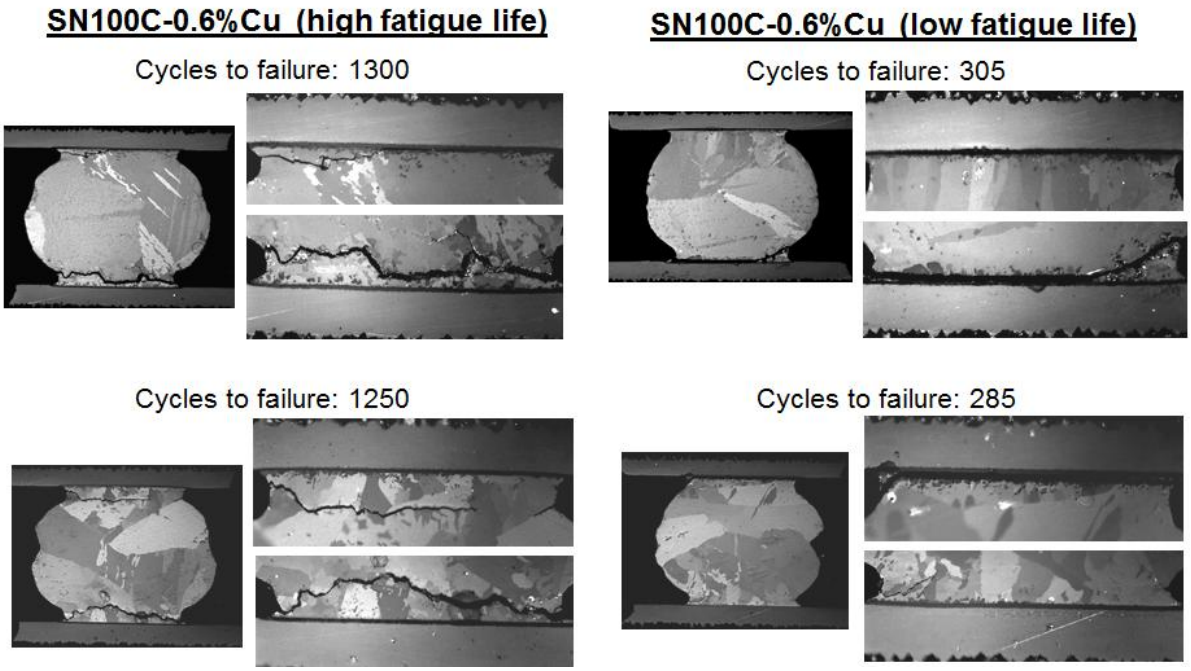


Figure 4.6: Failure modes for robust and fragile joints bonded to ENIG pads, from HSCBT tests.

4.3 Influence of bending frequency

Owing to the random IMC failures in solder joints on ENIG pads, a study on the influence of bending frequency was performed using joints on bare copper (OSP) pads only, in order to obtain consistent fatigue data and to maximize usage of the limited number of samples. Two solder materials were selected for this study, namely 1) SAC101, a commonly available lead-free solder which has good robustness under drop impact; and 2) SN100C solder provided by Nihon Superior

Pte Ltd, which is used for the solder joint life prediction work described later in Chapter 5. High speed cyclic bend tests at various PCB strain amplitude levels and frequencies were conducted to generate data to construct S-N curves that characterize fatigue failure.

Figure 4.7 shows the S-N curves for SAC101-Cu joints for frequencies ranging from 30 Hz to 150 Hz. The mean value for each dataset is indicated by a circular marker and the error bars correspond to one standard deviation. A detailed error analysis of each dataset is presented in Table D.2 of Appendix D. S-N curves are fitted to the data assuming a power law relation between PCB strain and the number of cycles-to-failure. The goodness of fit is indicated by the coefficients of correlation (R^2) in the graph. Among the common regression types (exponential, logarithmic, exponential, polynomial), a simple power law is found to give the best fit to the fatigue data, and avoids the complications of other more complex regression approaches. The fatigue life can be observed to decrease monotonically with PCB bending frequency.

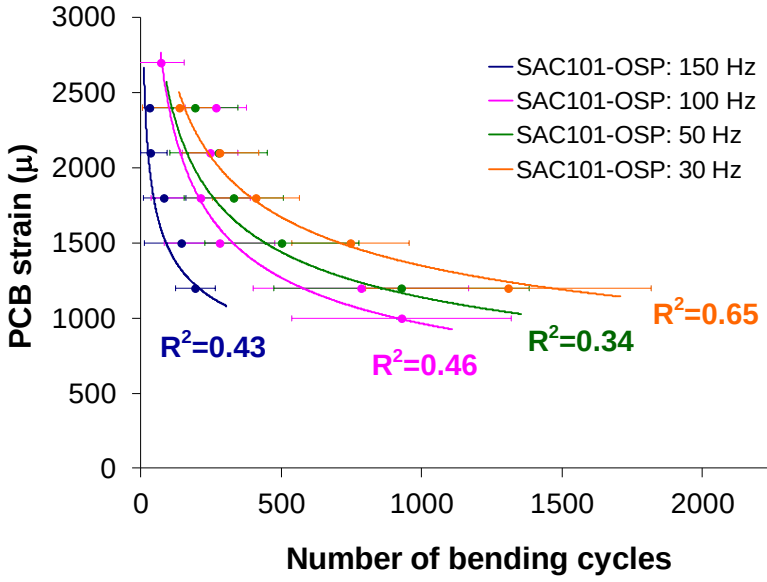


Figure 4.7: S-N curves for SAC101-Cu joints for various bending frequencies.

Figure 4.8 shows S-N curves for SN100C joints, for bending frequencies ranging from 50 Hz to 300 Hz. The graph shows all of the data points, and a detailed error analysis of the fatigue data is presented in Appendix D. While a linear fit may be adopted for the two strain levels in Fig. 4.8, a power law fit is used to maintain consistency with the results of Fig. 4.7, and with the widely-accepted power law relationships (e.g. Coffin-Manson) used in industry. As with the SAC101-Cu material system, SN100C-Cu joints exhibit strain rate sensitivity, where fatigue life decreases monotonically with PCB bending frequency. A major difference between the results for SAC101 and SN100C joints is that the S-N curves for SAC101 converge at higher PCB strains, suggesting a greater occurrence of random IMC failure across all frequencies at high strain amplitudes. The S-N curves for SN100C remain separate, even at high load amplitudes of 3000 microstrains.

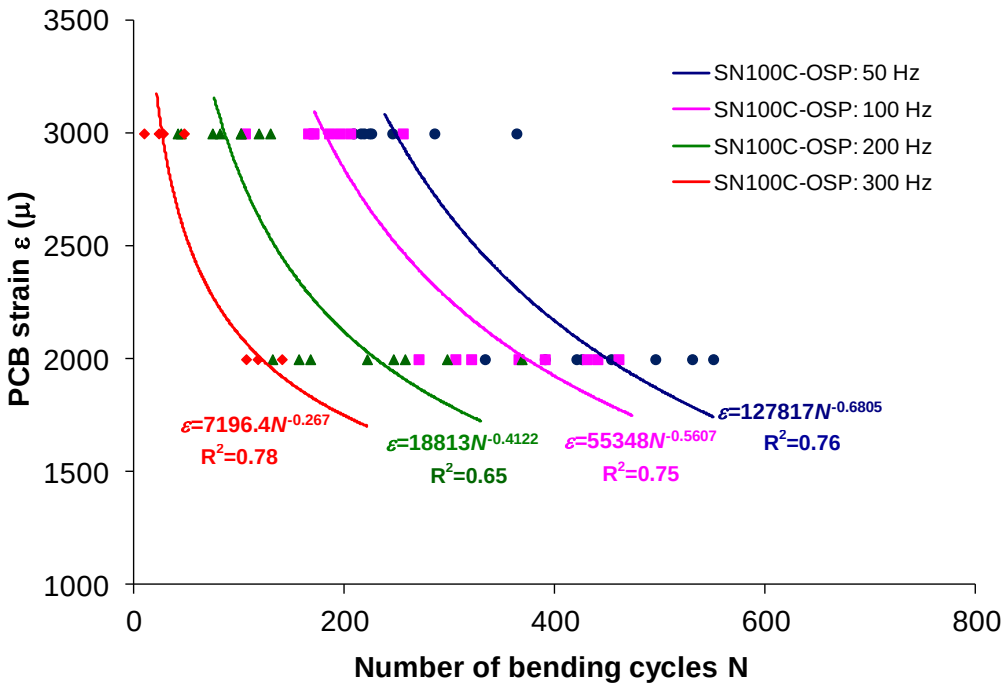


Figure 4.8: S-N curves for SN100C-Cu joints for various bending frequencies.

An examination of the fracture surfaces of samples tested at various frequencies provides an explanation for the considerable reduction of solder joint robustness at higher bending frequencies. Figure 4.9 shows a comparison between the fracture surfaces of SN100C solder joints tested at frequencies of 200 Hz and 300 Hz, for a strain amplitude of 3000 microstrains. The fracture surfaces for loading at 200 Hz have retained solder material, indicating the occurrence of ductile failure in the bulk solder. However, the fracture surfaces for 300 Hz exhibit a mostly smooth appearance, indicating that brittle failure has occurred along the IMC layers. The higher strain rates – generated by the higher bending frequency – have likely suppressed plastic deformation in the solder and promoted brittle IMC failures.

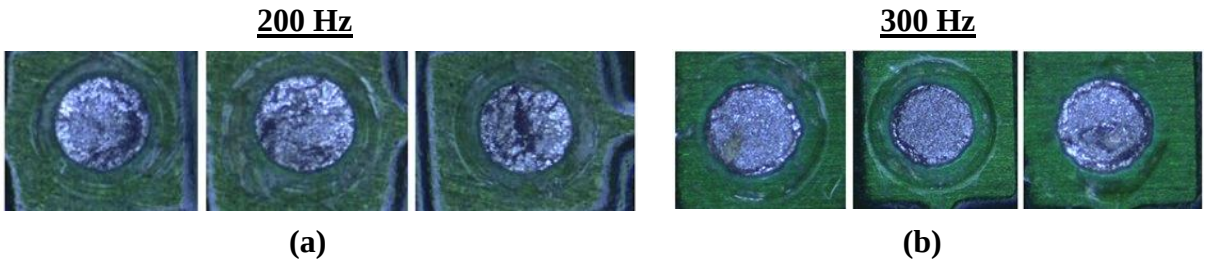


Figure 4.9: Fracture surfaces of SN100C joints for (a) 200 Hz, 3000 microstrains; (b) 300 Hz, amplitude 3000 microstrains

Transition from ductile to brittle failure is an intuitive explanation for the reduced fatigue life between 200 Hz and 300 Hz. It does not, however, explain the significant reduction in fatigue life between 50 Hz and 200 Hz, where the failure mode is predominantly bulk solder cracking over this frequency range. Figure 4.10 shows cross-sections of failed SN100C joints taken from 50 Hz and 200 Hz tests conducted at a PCB strain amplitude of 3000μ. Given that the 50 Hz and 200 Hz samples have very different fatigue lives yet exhibit predominantly bulk solder cracking, it is clear that an increase in bending frequency has an effect on the rate of crack propagation in the bulk solder. There is a noticeably high degree of crack

branching in the 50 Hz sample. The crack path also tends to become straighter as the frequency increases. For one of the 200 Hz samples (221 cycles to failure), there is mixed-mode fracture, where crack path alternates between the bulk solder and the IMC region. Therefore, shorter crack paths and mixed mode failure are hypothesized to be the reasons for the reduced fatigue life at higher bending frequencies.

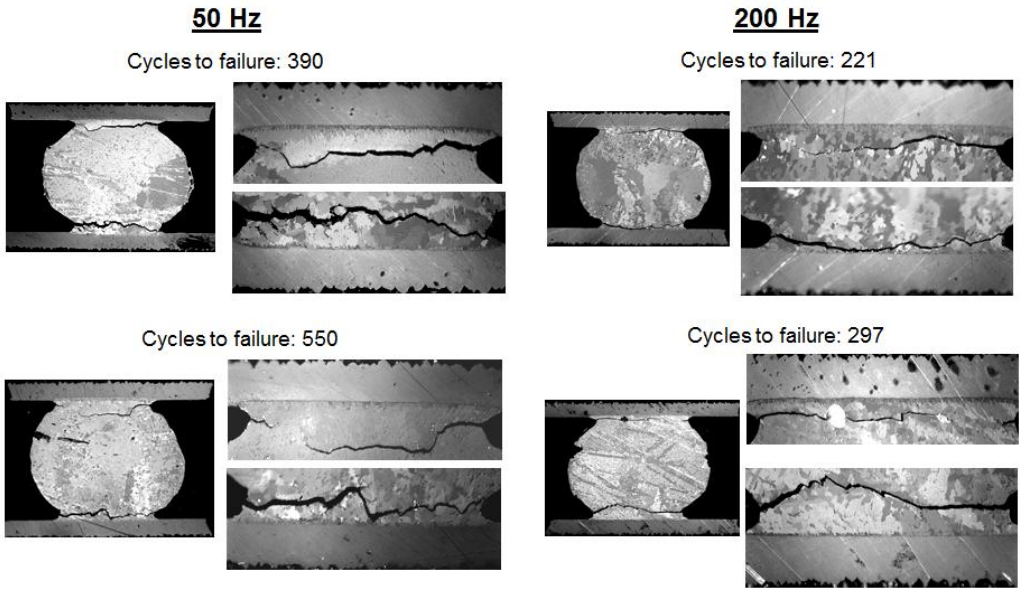


Figure 4.10: Failure modes for SN100C joints subjected to 50 Hz and 200 Hz PCB bending frequencies, at a 2000 microstrains amplitude.

From a practical perspective, the S-N curves generated in this study can be used by designers of portable electronic devices to avoid loading conditions that cause catastrophic interconnection failures, or to engineer the devices to sustain a prescribed number of load cycles. To preclude sudden failures, designers should avoid amplitude and frequency combinations which produce brittle IMC failures such as those shown in Fig. 4.9(b). For certain materials, care should also be taken to avoid exceeding particular bending frequencies. For example, the 150 Hz curve for SAC101-Cu(OSP) in Fig. 4.7 shows low cycles-to-failure across a wide range

of amplitudes. While low PCB natural frequencies will generally result in higher cycles-to-failure, a high strain amplitude may negate this advantage, as seen in the convergence of the SAC101-Cu(OSP) data in Fig. 4.7 at high amplitude levels. For mobile phone applications, a designer is likely to be concerned with only the leftmost portion of the S-N curves that represent cycles-to-failure of less than 100, since few users are expected to drop their devices excessively repeatedly. However, it should be noted that if damping is lacking in the device, each drop can result in a large number of load cycles. The right side of these S-N curves are more relevant to situations where continuous impacts or resonant vibration occur, such as in machinery and vehicular applications.

4.4 Influence of temperature

Given the increased brittleness of solder joints at higher strain rates, it is hypothesized that that a temperature reduction would have an effect similar to that of increased bending frequency, and lower the fatigue life. The experimental setup for studying the effect of temperature is shown in Fig. 4.11. Liquid nitrogen is directed onto the component through a flexible hose. A thermocouple placed on the component measures the local temperature at the component and its solder joints. A temperature controller maintains the temperature at the prescribed level using a hot air blower attached in series with the liquid nitrogen line. The fatigue life results for room temperature and 0º C, for a strain amplitude and frequency of 2000μ and 100 Hz respectively, are shown in Fig. 4.12. No significant differences are observed between the fatigue results at room temperature and 0º C.

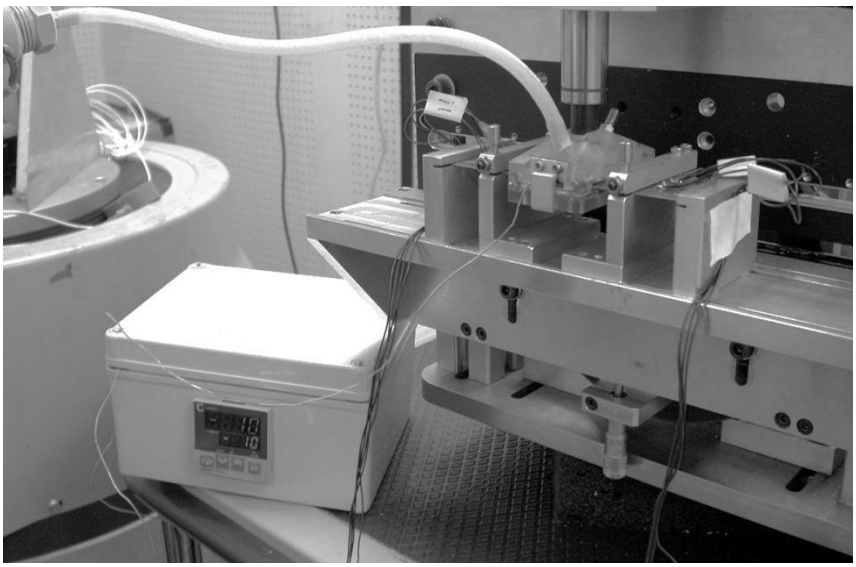


Figure 4.11: Low temperature test setup on high speed cyclic bend tester.

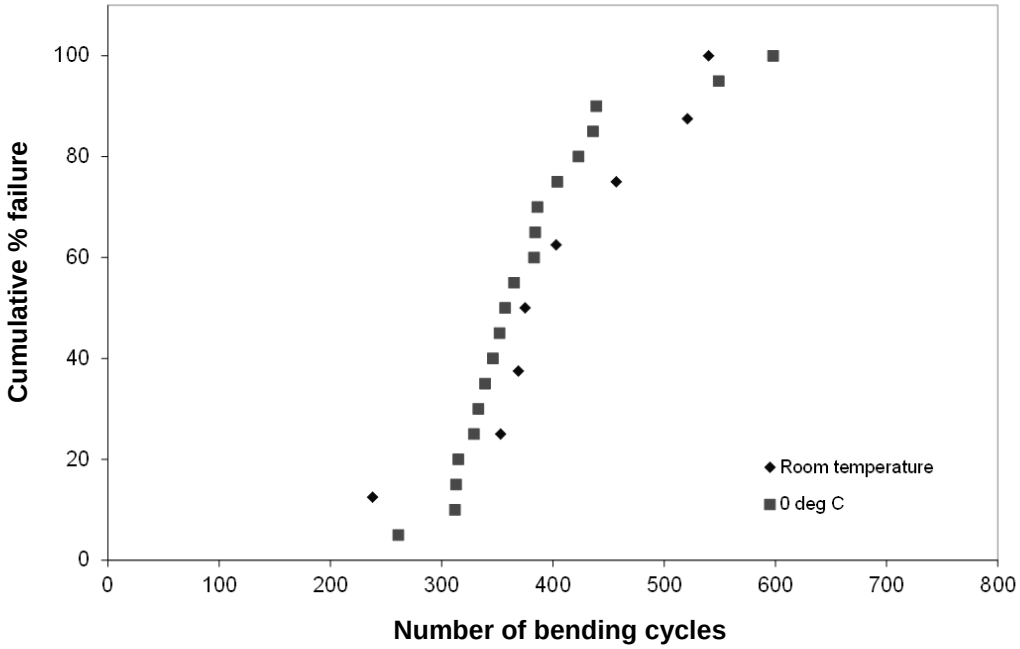


Figure 4.12: HSCBT test life for SN100C-Cu joints at two temperatures (100 Hz frequency, 2000 microstrain amplitude).

To further investigate the effect of temperature, several additional tests were performed to determine if there is a ductile-to-brittle transition temperature for solder joints. For these additional tests, an extremely low temperature of -30ºC and a high PCB amplitude of 3000 microstrains were used as test conditions. At the request of an industry collaborator, an additional solder material, LF35 (Sn-1.2Ag-0.5Cu) was also tested. Figure 4.13 shows the S-N curves for the two solder joint material systems tested, under room temperature and -30º C conditions. The solid lines are the room temperature S-N curves, while the dashed lines are the -30ºC S-N curves. A low temperature of -30º C does not cause a change in robustness for low PCB strains (2000μ) for both materials. However, for high PCB strains, a reduced temperature has a dramatic effect on the robustness of the joints, as indicated by the divergence between the solid and dashed lines at high strains. These results show that there is a threshold temperature at which joints become fragile, and this effect is exacerbated by high strains.

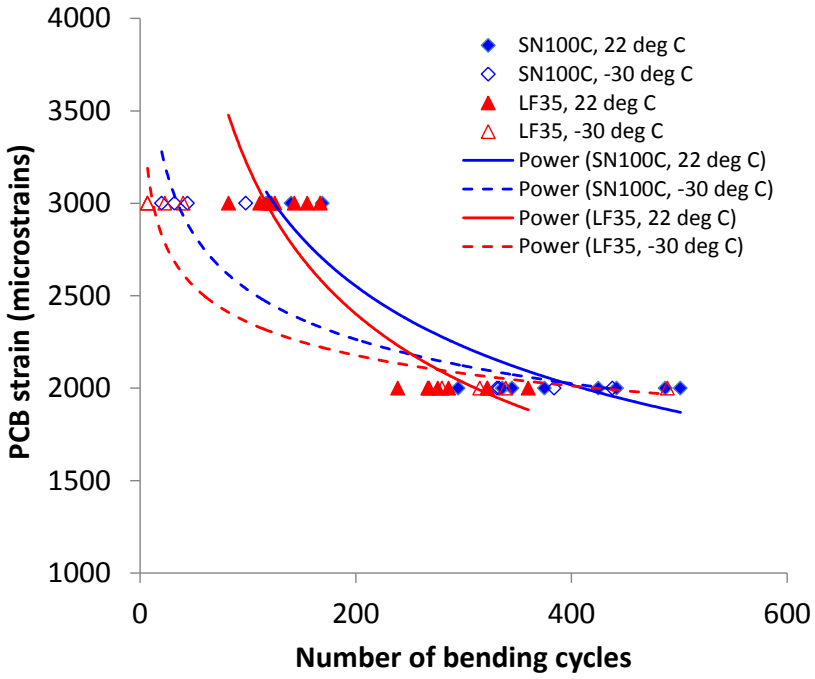


Figure 4.13: S-N curves for SN100C and LF35 on bare copper pads, for room temperature and -30º C.

4.5 Effect of Loading Sequence

4.5.1 Introduction

The fatigue lives of solder joints described in the preceding sections were obtained for conditions of constant PCB strain. In an actual system level drop test, the load history consists of highly variable strain amplitudes. If fatigue life is affected by the order in which the constituent amplitudes are applied, then there is a sequence effect. As an illustration, consider a JEDEC board level drop test which produces a unique variable load history, shown in Fig 4.14(a). Figure 4.14(b) shows the exact same load history, but reversed in sequence. If the damage caused by these two load histories are different, then a load sequence effect exists.

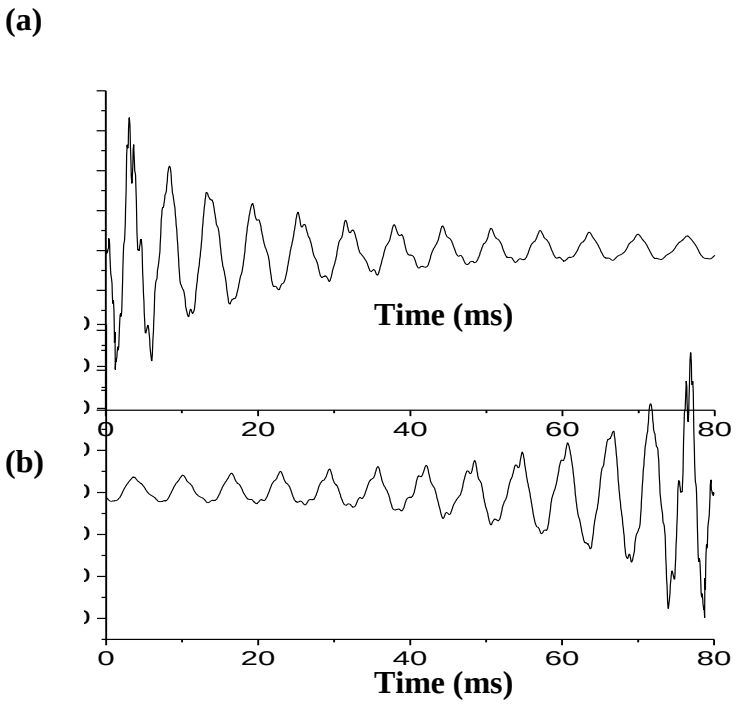


Figure 4.14: (a) Typical strain history in a JEDEC board level drop test; (b) Similar strain history, but reversed in sequence.

The most basic model for determining damage caused by a variable amplitude load history is the Palmgren-Miner Rule [22], which assumes that the damage due to a variable load history is a linear summation of the damage caused by its constituent amplitudes. The Palmgren-Miner rule is illustrated graphically in Fig. 4.15(a), where the test specimen is subjected to multiple load amplitudes ε_i for corresponding numbers of cycles n_i. Each load cycle at a given amplitude ε_i is assumed to cause a fixed amount of damage $1/N_i$., where N_i is the number of cycles-to-failure at that amplitude; note that N_i defines points along the S-N curve. Each load amplitude therefore consumes a portion of the specimen fatigue life, given by the ratio n_i/N_i. The Palmgren-Miner Rule calculates damage – also known as "Miner's Sum" – according to the following equation:

$$\text{Damage, } D = \sum \frac{n_i}{N_i}$$

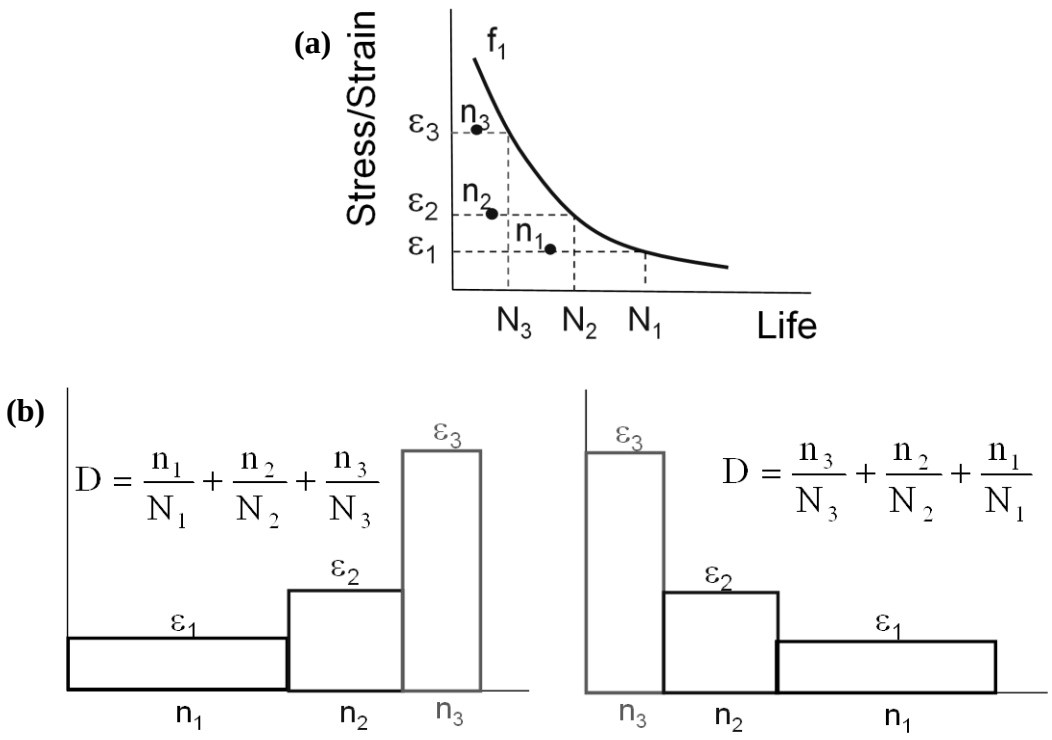


Figure 4.15: Illustration of the use of the Palmgren-Miner rule: a) Each block of load amplitude ε_i consumes a fraction of the fatigue life, n_i/N_i. (b) The rule assumes no sequence effect.

A value of D=1 defines failure of the specimen according to the Palmgren-Miner Rule for damage accumulation. The rule disregards the effect of load sequence; therefore various permutations of a given set of load amplitudes – as illustrated in Fig. 4.15(b) – are assumed to produce the same level of damage in a test specimen.

The methodology used in this load sequence investigation is to calculate D for various load sequences on the solder joints. Deviation from D=1 at failure indicates that there is a sequence effect. For example, D<1 at failure indicates that the joint has failed earlier than predicted by the Palmgren-Miner model, and that the load sequence imposed has a detrimental effect on solder joint fatigue life.

4.5.2 Study of sequence effect for two constant amplitude blocks

The first type of load sequence investigated is one with two load blocks, where a series of load cycles at constant amplitude are applied to the solder joint, followed by a series of load cycles at a different amplitude, until the solder joint fails. Figure 4.16 illustrates two sequences studied. The first has a low (L) amplitude block followed by a high (H) amplitude block, while the second has an H block followed by an L block. L and H amplitudes correspond to 1200 and 1800 microstrains respectively, measured on the PCB adjacent to the component. The solder material system is SAC101-Cu. The damage sum is calculated for these load histories using the Palmgren-Miner rule.

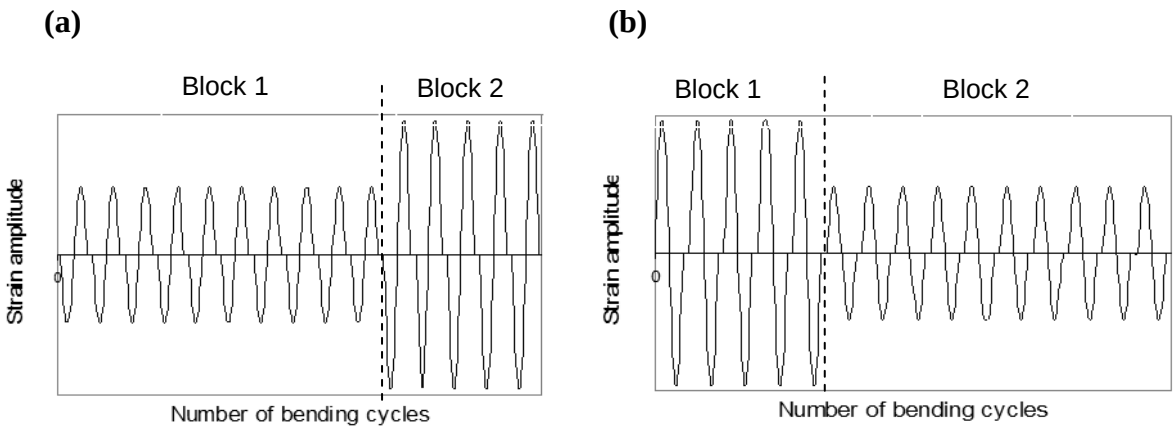


Figure 4.16: Sequences with two load blocks: (a) Low amplitude block, followed by a high amplitude block; (b) High amplitude block followed by a low block.

To obtain meaningful results, it is necessary to manage the problem of data scatter, which is typical of fatigue experiments; examples of data scatter can be seen in the results presented in Section 4.3, where the data is spread over a range centered on the S-N curve. Consequently, the damage sum or parameter D will also exhibit a similar level of scatter, because the S-N curves that define N_i are used to calculate D. For example, a weak solder joint with a nominal fatigue life that is lower than the S-N fit will yield a D value smaller than unity.

To address this data scatter problem, the crack growth rate in the first block is used to estimate the nominal fatigue life of individual joints (or whether they are weaker or stronger than average). In Block 1, the crack is increased to at least 30% of the cross-sectional area. The nominal fatigue life corresponding to the Block 1 strain amplitude ε_1, is estimated by extrapolating the crack area in Block 1 to 100% of the cross-sectional area; this method is based on the assumption that cracks which grow fast initially tend to maintain their rapid crack growth up to failure. This assumption is supported by the typical crack growth characteristics shown in Figs.

4.17 and 4.18. The relative robustness of a joint (compared to the average) is determined by its position within the scatter band. To obtain the nominal fatigue life associated with the strain amplitude ε_2 in Block 2, the corresponding position within the scatter band for ε_2 is located. The blue dots in Fig. 4.19 illustrate an example of a sample which has a nominal fatigue life that is in the middle of the scatter band; the nominal N_i for this sample are 288 and 520 cycles respectively, for H and L amplitudes.

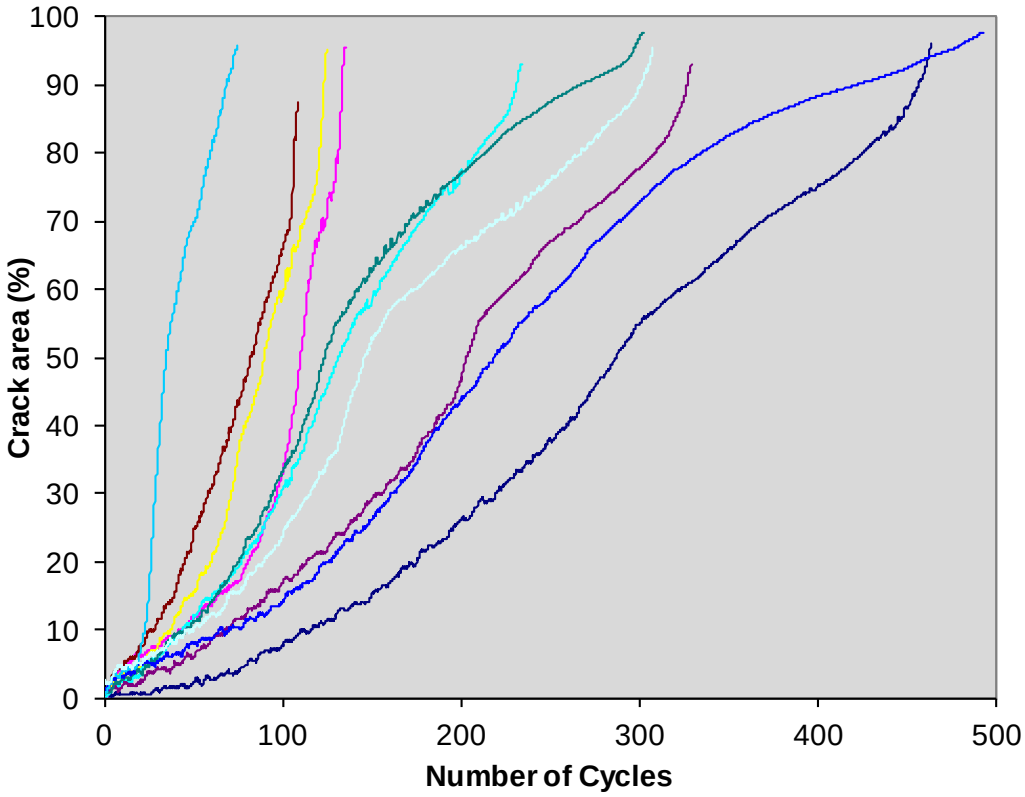


Figure 4.17: Constant amplitude crack growth curves at L amplitude. Each curve represents crack growth in a particular solder joint.

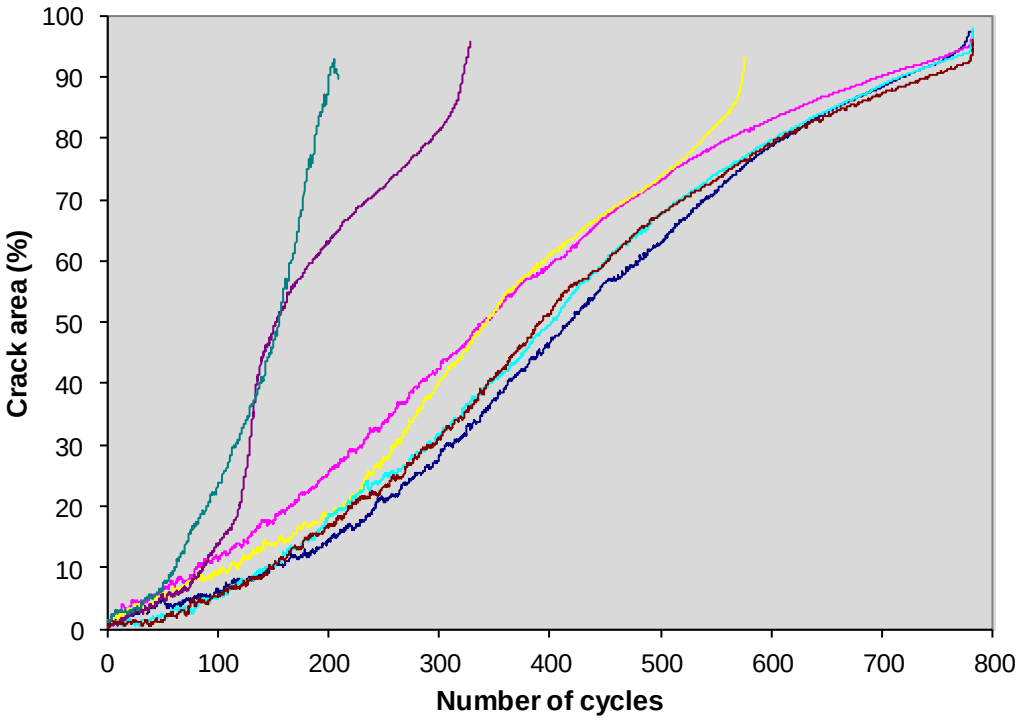


Figure 4.18: Constant amplitude crack growth curves at H amplitude. Each curve represents crack growth in a particular solder joint.

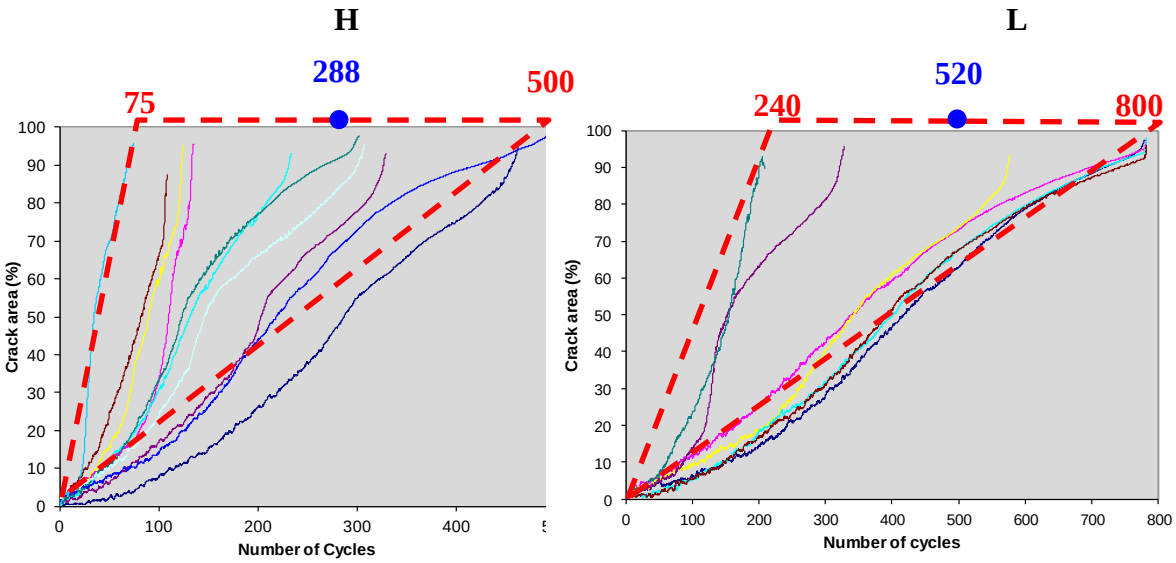


Figure 4.19: Scatter bands for H and L constant amplitudes.

Table 4.2: Damage parameters for L-H two-block sequence tests

	N_1 (cycles)	N_2 (cycles)	n_1 (cycles)	n_2 (cycles)	Crack in 1st block (%)	D
Sample 1	800	500	239	114	28	0.53
Sample 2	646	383	213	144	33	0.71
Sample 3	532	297	202	111	38	0.75
Sample 4	769	477	300	207	39	0.82
Sample 5	352	160	140	41	40	0.65
Sample 6	725	443	332	135	46	0.76
Sample 7	800	500	427	136	52	0.81
Sample 8	387	186	213	129	55	1.24
Sample 9	360	166	202	72	56	0.99
Sample 10	470	249	266	103	57	0.98
Sample 11	655	390	414	75	63	0.82
Sample 12	385	185	247	57	64	0.95
Sample 13	364	169	247	50	68	0.97
Average D ± standard deviation						0.84 ± 0.18

Table 4.2 shows the results for the L-H load sequence experiments. Constant amplitude cyclic loading lives N_i and block cycles n_i used for calculation of D are shown; the crack growth in the first step ranges from approximately 30% to 60%. The linear damage sum D is consistently below unity for almost all samples. Crack growth curves for the L-H tests are shown in Fig. 4.20. The transition point between Block 1 and Block 2 can be identified as a kink in the crack growth curve, examples of which are indicated by the red arrows on the graph. The crack growth at the transition points provides a clue as to why D is smaller than unity. Immediately after the transition points, the curves show a steep gradient, indicating

a rapid growth rate. The gradient gradually decreases as the H load cycles continue.

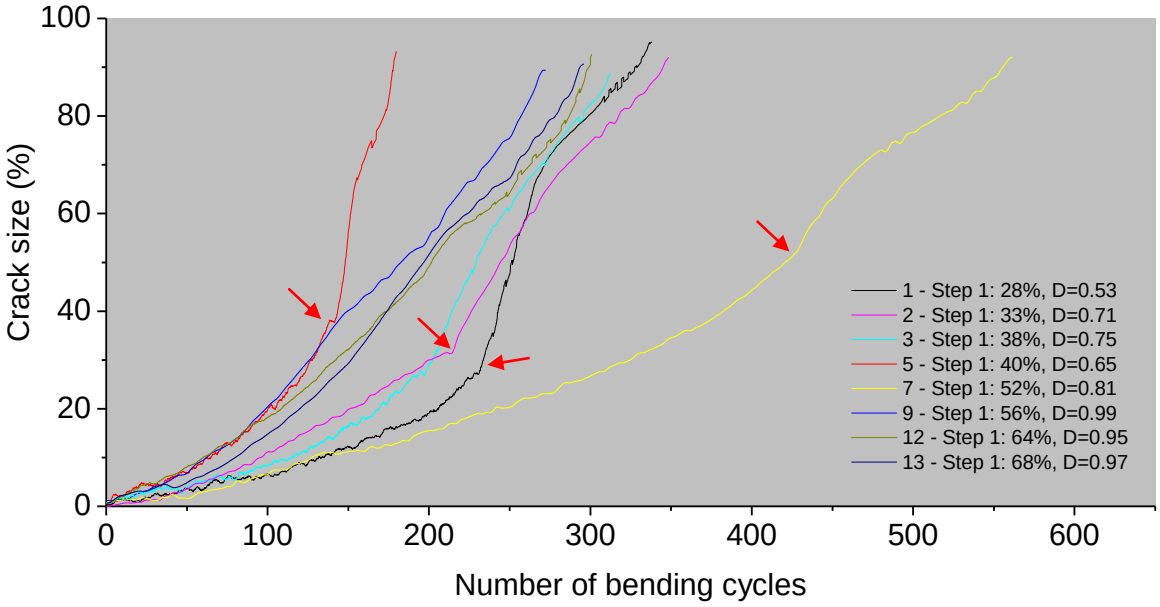


Figure 4.20: Crack growth curves for L-H tests.

Table 4.3 shows the results for the reversed two-block sequence, or H-L tests. The values of the linear damage sum D at failure shows a much more even spread about unity than the L-H tests. Corresponding crack growth curves are shown in Fig. 4.21.

Summarizing the results of this two-block sequence study, it is observed that L-H transitions have a detrimental effect on fatigue life, while H-L transitions did not exhibit significant sequence effects. Both observations were unexpected; H-L transitions were envisaged to result in D values larger than 1, based on conventional theory that residual stresses remaining from high loads cause crack closure in the region around the crack tip [52]. The linear damage sums are in any case small deviations from unity, perhaps owing to the presence of only a single

load transition. We next study the effect of multiple load transitions, to determine if the deviations – especially that due to the L-H sequence effect – are correspondingly amplified.

Table 4.3: Damage parameters for H-L two-block sequence tests

	N_1 (cycles)	N_2 (cycles)	n_1 (cycles)	n_2 (cycles)	Crack in 1st block (%)	D
Sample 1	500	800	110	546	22	0.90
Sample 2	481	776	130	400	27	0.79
Sample 3	281	512	90	263	32	0.83
Sample 4	194	397	70	53	36	0.49
Sample 5	234	449	97	336	41	1.16
Sample 6	137	322	60	193	44	1.04
Sample 7	290	523	137	183	47	0.82
Sample 8	462	751	259	473	56	1.19
Sample 9	482	776	270	252	56	0.88
Sample 10	172	367	108	100	63	0.90
Sample 11	171	366	108	137	63	1.01
Sample 12	193	395	130	94	67	0.91
Average D ± standard deviation						0.91 ± 0.19

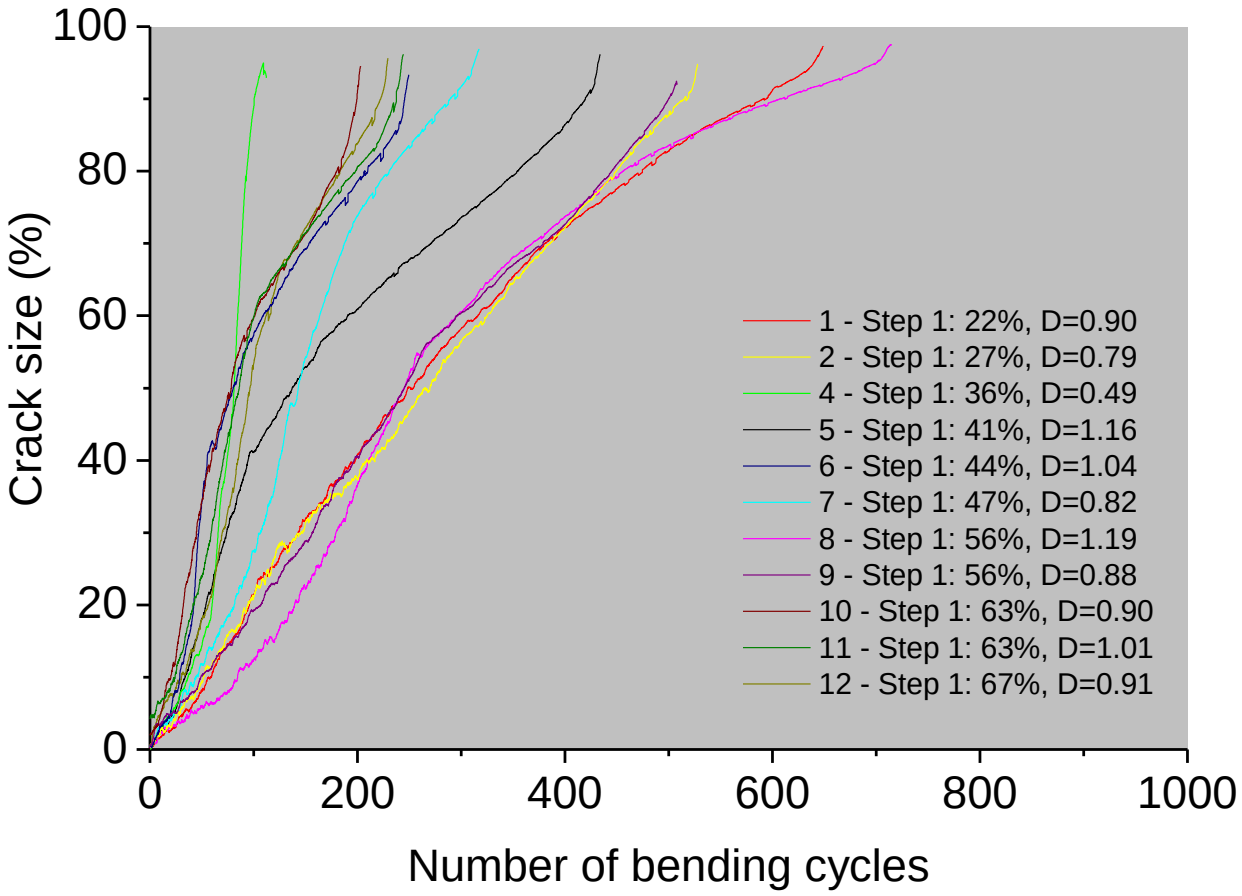


Figure 4.21: Crack growth curves for H-L tests.

4.5.3 Study of L-H sequence effect for multiple alternating blocks

In this study, solder joint samples are first cycled at an L amplitude – to a crack size of at least 30% to determine N_i – followed by alternating H and L blocks of 40 load cycles each. Figure 4.22 shows the crack growth curve for a solder joint sample. L-H transition points are indicated by blue arrows, and H-L transition points by green arrows. Note the relatively high gradients immediately after the L-H transition points.

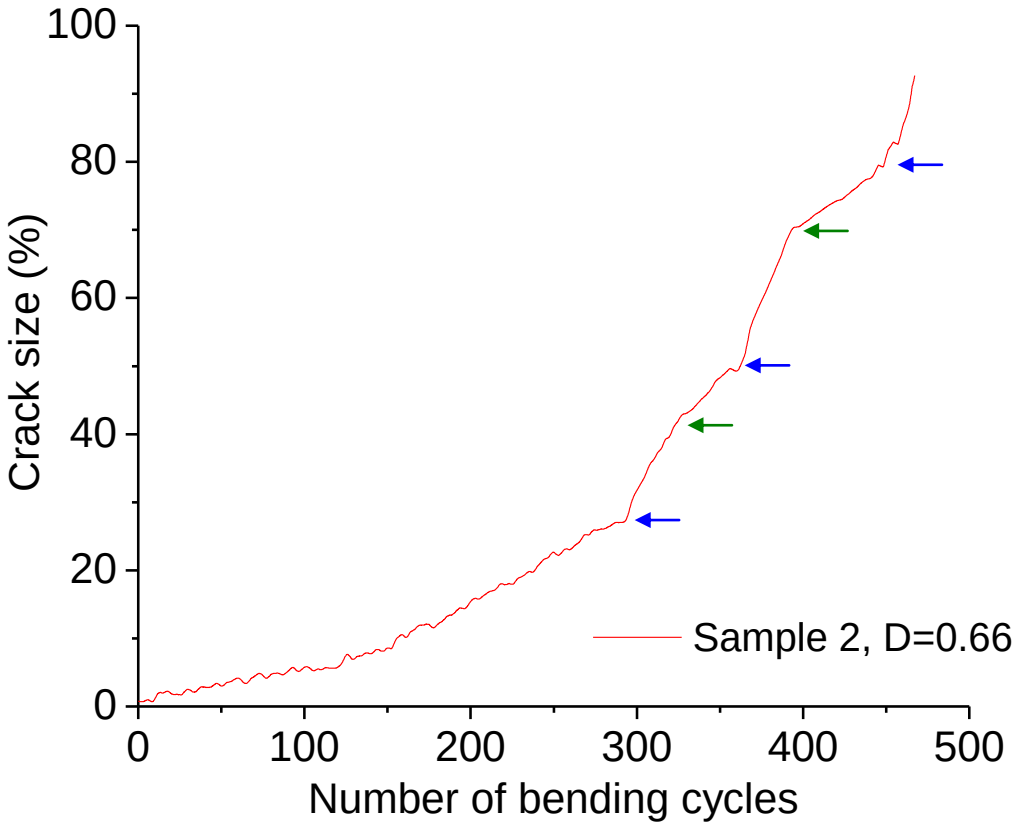


Figure 4.22: Crack growth curve for multiple load blocks

Table 4.4 shows the linear damage sums for the 5 samples tested in this study. While still lower than unity, the D values for the multiple block tests are only slightly smaller than those of the two-block L-H tests; the sequence effect in the multiple block tests is not a linear multiple of the sequence effect seen in an L-H test.

Table 4.4: Damage parameters for multiple block tests

	Component, n_i/N_i				
Sample / Block	**1**	**2**	**3**	**4**	**5**
1	0.322	0.365	0.338	0.170	0.120
2	0.064	0.072	0.072	0.093	0.060
3	0.051	0.040	0.049	0.069	0.049
4	0.058	0.070	0.062	0.130	0.084
5	0.048	0.053	0.049	0.067	0.048
6	0.064	0.058	0.084	0.106	0.068
7			0.049	0.065	0.046
8			0.072	0.124	0.080
9			0.042		0.046
10			0.032		0.056
11					0.090
D	**0.61**	**0.66**	**0.85**	**0.82**	**0.69**

4.5.4 Study of complex load sequences

For a more comprehensive survey of load sequence effects in drop impact, several additional sequence patterns were examined; these are depicted in Fig. 4.23. It should be noted that these depictions of sequence patterns are schematic representations of the variable loads applied. Although the sequences are depicted as continuous, in reality there is a duration of no load between bending cycles, as a result of the design of the high speed bend tester (see Appendix C). A Type A load sequence consists of alternating blocks where each block consumes approximately 5% of the constant amplitude life; this sequence is similar to that described in the previous section, but with more blocks. A Type B load sequence assesses the effect of a single overload cycle on fatigue failure. A Type C load sequence consists of alternating individual pulses of different amplitudes, to generate the maximum possible number of load transitions. A Type D load sequence has a progressively increasing and decreasing series of loads, in order to study the effect of directionality and step size.

In this study, SN100C-Cu samples were used, as they exhibit very small data scatter. The constant amplitude fatigue life N_i used for calculating the damage sums is obtained from the S-N data fit. The bending frequency is fixed at 100 Hz. Three load amplitudes are used for the variable load histories; these are denoted by L (2000 microstrains), M (3000 microstrains) and H (4000 microstrains), and the corresponding N_L, N_M and N_H are determined from the S-N data in Fig. 4.8.

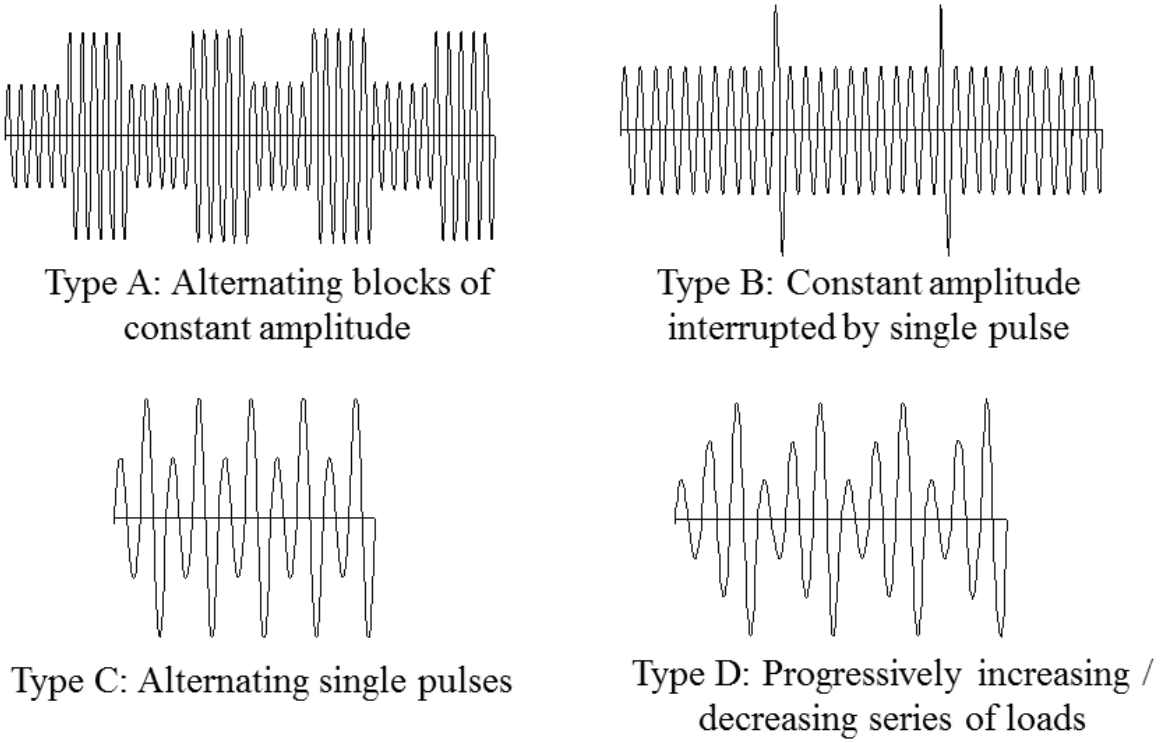


Figure 4.23: Complex load sequences studied.

Table 4.5 shows the calculated damage for samples corresponding to load sequence Type A. The damage sum D is consistently less than unity for most of the samples, which is expected, based on similar multiple-block tests on SAC101-Cu samples presented in Section 4.5.3.

Table 4.5: Damage sums for Load Sequence A

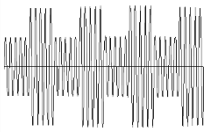
Load sequence 	**D**	**Average D**
L–H–L–H…	0.64, 0.82, 0.81, 0.78, 1.06, 0.95, 0.81, 0.92	0.85
M–H–M–H…	0.86, 0.85, 1.14, 0.74, 0.44, 0.40, 0.81, 0.74	0.75
L–M–L–M…	0.81, 0.97, 0.91, 0.87, 0.87, 0.81, 0.92, 0.81	0.87

Table 4.6 shows the calculated damage for samples tested according to load sequence Type B. This sequence consists of a constant amplitude test which is interrupted – at intervals of approximately 5% fatigue life – by single sinusoidal bending pulses of a larger amplitude. The samples for L constant amplitude with H interruptions ("L, single H" sequence) show a significant improvement in fatigue life, where D exceeds unity for most samples tested. The improved fatigue performance is likely due to the H amplitude causing yielding and residual stresses around the crack tip, resulting in a degree of crack closure which has to be overcome by subsequent L amplitude loading before the crack can advance. This crack closure phenomenon does not appear to occur for the "M, single H" sequence in Table 4.6, possibly because the difference in amplitude between M and H is too low. This may also explain why crack closure effects were not observed in the H-L two-block sequence tests discussed in Section 4.5.2.

Table 4.6: Damage sums for Load Sequence B

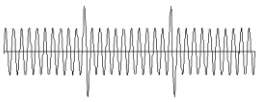
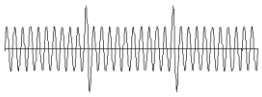
Load sequence		D	Average D
L, single H		1.05, 0.96, 1.07, 0.97, 0.84, 1.42, 1.29, 1.39	1.12
M, single H		1.06, 0.81, 1.23, 1.02, 0.30, 1.00, 0.98, 0.89	1.00

Table 4.7: Damage sums for Load Sequence C

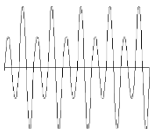
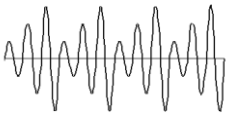
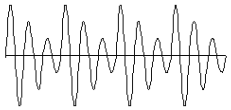
Load sequence 	**D**	**Average D**
L–H–L–H…	**0.34, 0.52, 0.62, 0.80, 0.35, 0.88, 0.95**	**0.64**
M–H–M–H…	**0.63, 0.55, 0.83, 1.02, 0.4, 1.06, 1.12**	**0.80**
L–M–L–M…	**0.60, 0.74, 0.88, 0.51, 0.88, 0.94, 0.83**	**0.77**

Table 4.7 shows the calculated damage for a Type C load sequence, with single alternating cycles. The average D value for this sequence is not much lower than unity despite the large number of transitions. L-H-L-H and M-H-M-H sequences show a large scatter owing to the dominance of the H amplitude in contributing to the damage and causing mixed mode failures.

Table 4.8 shows the calculated damage for progressively increasing or decreasing sequences of L, M and H amplitudes. Both sequences give D values close to unity.

Table 4.8: Damage sums for Load Sequence D

Load Sequence		D	Average D
L–M–H		0.88, 0.94, 0.86, 1.01, 1.16, 1.00, 1.09	0.99
H–M–L		0.72, 0.72, 0.81, 0.86, 0.88, 0.91, 1.01, 1.05	0.87

4.6 Summary and conclusions

A series of studies were undertaken to investigate various parameters that influence the fatigue failure of solder joints under dynamic PCB bending. Solder material and pad finish have a strong influence on the bending amplitude and/or frequency at which transition between ductile bulk solder failure and intermetallic compound (IMC) failure occurs. Of all the materials tested, SAC101 exhibits the most robust performance, while SAC305 has the poor robustness under dynamic PCB bending. ENIG pad finish promotes brittle IMC failure under dynamic loads for all the materials tested. The PCB bending frequency has a major influence on the robustness of the joints. There is a monotonic decrease in joint robustness with bending frequency. At higher bending frequencies, there is increased occurrence of IMC or mixed mode failures. At lower bending frequencies, crack propagation paths are observed to be more erratic and exhibit more branching. A limited study on temperature effects was also performed. A reduction in temperature from room temperature to 0º C does not cause a significant change in SN100C-Cu solder joint robustness for the test amplitude (2000 microstrain) and frequency (100 Hz) imposed. However, at high strains (3000 microstrains) and under very low temperatures (-30ºC), a significant reduction in robustness is observed. For practical application, designers of electronic devices can use these fatigue characteristics to engineer products to exclude amplitude/frequency combinations that cause catastrophic IMC failure, or to ensure that products can survive given load histories.

Studies on the effect of fatigue loading sequence were performed, using the Miner-Palmgren Rule for linear damage summation. Examination of load sequence

effects based on a basic two-block sequence reveals an interesting phenomenon; the crack growth rate is unusually high immediately after the transition from a low load amplitude to a high load amplitude. Studies using multiple load blocks also indicate the same phenomenon. The imposition of occasional high loads is found to improve fatigue life slightly, as is expected, because of the generation of residual stresses at the crack tip by the overload, resulting in crack closure. In all the studies that were performed on load sequence effects, the linear damage sum for the majority of samples was within 20% of D=1, indicating that when they do occur, sequence effects are minor.

Chapter 5

Fatigue Modeling and Life Prediction

This chapter describes the development of fatigue models for predicting whether solder joints will fail under given combinations of load amplitude and frequency. Two models are proposed. The first involves basic curve fitting of the S-N data obtained from dynamic bending tests; this rudimentary model is straightforward and practical for industry use, but does not capture the physical mechanisms of fatigue failure. The second model is based on a proposed embrittlement function, which captures the combined effect of strain rate and strain amplitude in reducing fatigue life.

5.1 Introduction

Challenges in developing a drop impact life prediction model arise from: 1) complex load histories at the system/product level; and 2) a lack of effective test methods that can characterize fatigue under the high PCB bending strains and frequencies associated with drop impact. As discussed in Appendix C, the standard drop test method used in industry bears little resemblance to actual drop impacts of portable electronic devices, owing to the fact that the variable load history generated in a board-level drop test is different from that generated in a system level drop test. A further challenge arises from load sequence effects; however, for practical reasons, load sequence effects are ignored, based on the findings of Section 4.5, which show that the Palmgren-Miner damage sums remain close to unity for the wide range of load sequences examined.

The fatigue models discussed in Sections 5.2 and 5.3 of this chapter are essentially a consolidation of the experimental fatigue data that has been generated in this study. Each fatigue model has the form of a unified equation from which constant amplitude fatigue life can be derived. The fatigue models are used in conjunction with the Palmgren-Miner rule to predict fatigue life for complex load histories with varying amplitudes and frequencies. The last section of this chapter (Section 5.5) presents validation experiments designed to study limitations in the applicability of the fatigue models.

5.2 Fatigue Model 1: Curve fitting of S-N data

The S-N curves for various bending frequencies (SN100C-Cu material system) are plotted using logarithmic axes in Fig. 5.1. Because of the assumed power law relationship between PCB strain ε and the number of cycles-to-failure N, the curves are straight lines on a logarithmic scale. The S-N data exhibits two characteristics: 1) N decreases monotonically with frequency f; and 2) at higher strains, the decrease in N with f is several times higher than that at lower strains. The combination of high strain and high frequency has a compound effect in reducing fatigue life, which is manifested by a higher degree of IMC failure. A fatigue model must capture these frequency- and strain-dependent trends.

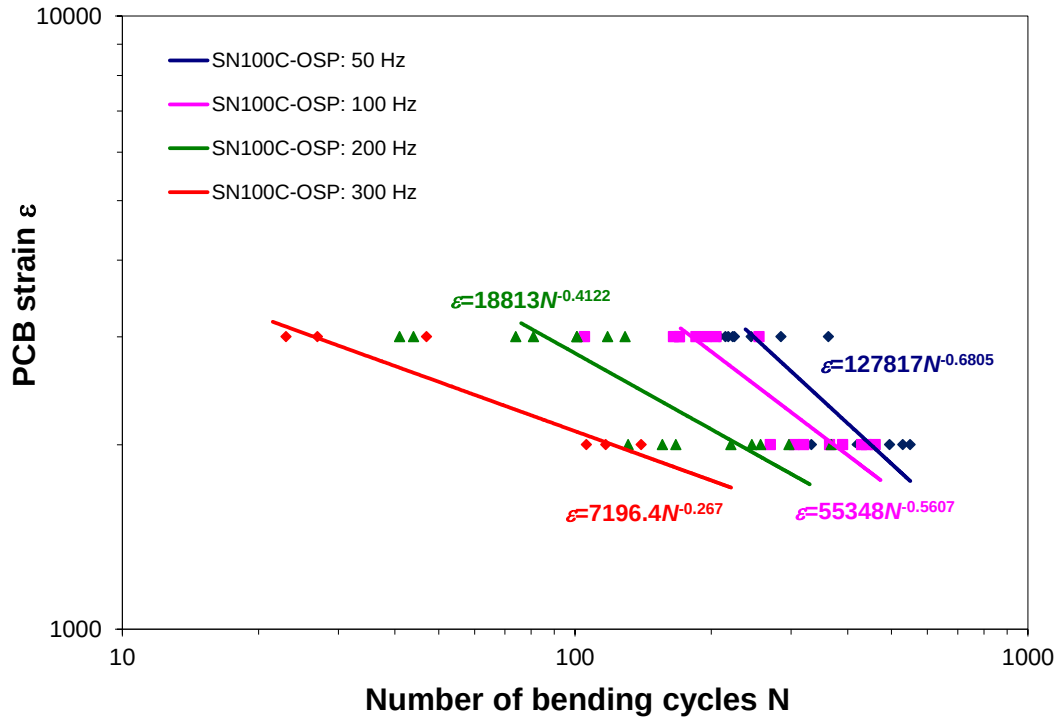


Figure 5.1: S-N curves for the SN100C-Cu material system.

In order to quantify changes in N with frequency and strain, fatigue life data is normalized with respect to the 50 Hz fatigue life, and plotted against bending frequency in Fig. 5.2; the ordinate of the graph is therefore the non-dimensional fatigue life expressed as a fraction of the 50 Hz fatigue life. Curve fits for each strain level are plotted as solid lines; each curve therefore indicates the variation of fatigue life with frequency for a particular strain level, and is defined by an exponential relation between the normalized fatigue life N' and frequency f:

$$N' = ce^{df} \tag{5.1}$$

where c and d are constants for a particular strain amplitude. An exponential relationship is assumed because it provides an excellent fit to the data, as shown in the high correlation coefficients indicated in Fig. 5.2.

The exponential curves shift to the left with increasing PCB strain, and broadly capture the observed trends. As the frequency increases, the curves flatten and approach zero, which essentially implies one cycle-to-failure; this reflects catastrophic brittle IMC failure at very high strain rates. For large strain amplitudes, the decrease in fatigue life with frequency is steep, due to the combined effect of high strain and high frequency in causing brittle IMC failures. For small strains, the gradient is gentler, which implies a more gradual ductile-to-brittle transition with frequency. Figure 5.3 shows the change in the exponential fit constants with PCB strain. A linear relationship between the constants and PCB strain is assumed.

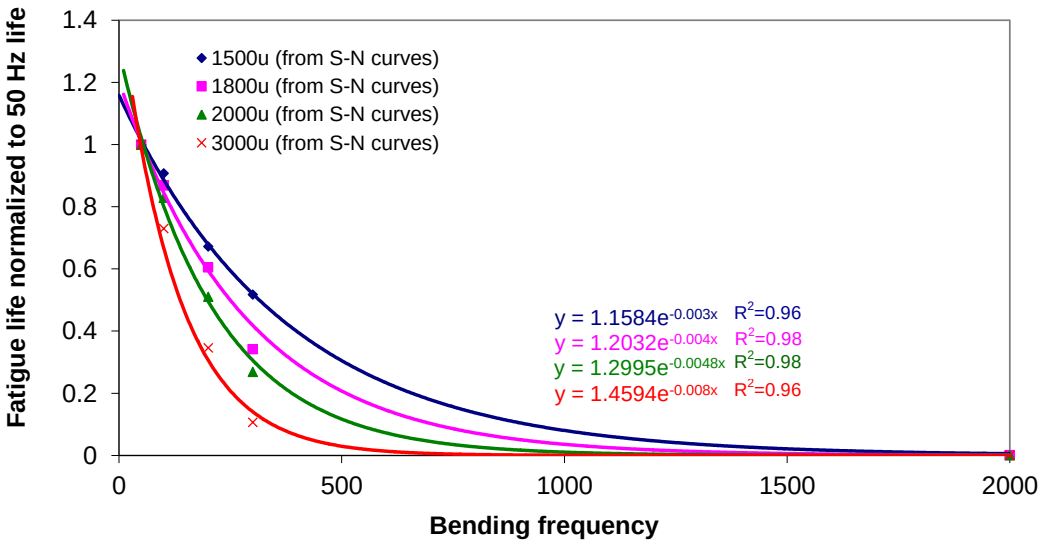


Figure 5.2: Variation of fatigue life with bending frequency, normalized with respect to 50 Hz data.

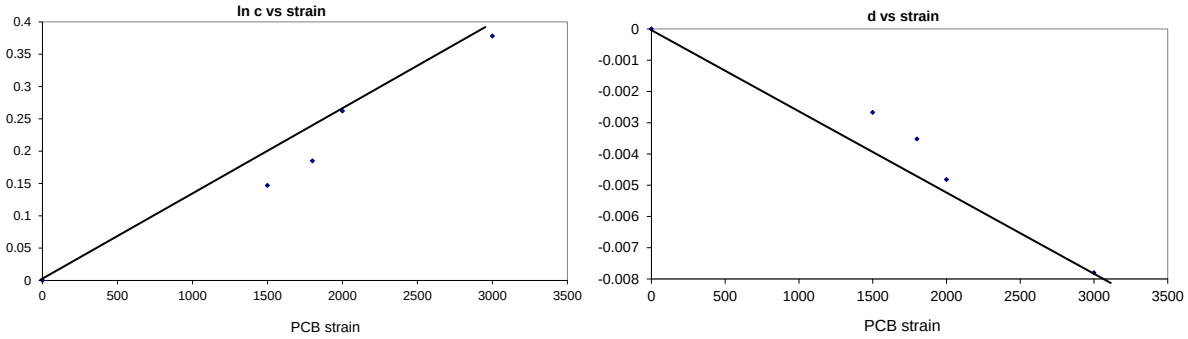


Figure 5.3: Variation of exponential fit constants with PCB strain amplitude.

The fatigue data is consolidated into a single equation, defined by:

$$N = a\varepsilon^{b}e^{\varepsilon(c+df)} \tag{5.2}$$

where

N is the cycles-to-failure, ε the PCB strain, f the bending frequency, a and b are power law constants for the reference curve, and c and d constants for the exponential fit.

The constants for SN100C-Cu joints, using the 50 Hz curve as baseline, are shown in Table 5.1. As the consolidated equation is obtained from a limited range of data (flexural frequency of 50 to 300 Hz; strain amplitude of 2000 to 3000 microstrains), care should be taken when using it to predict cycles-to-failure for strain/frequency combinations that are far beyond the empirical data used to fit the equation. Figure 5.4 shows S-N curves generated from the consolidated model, plotted with the original empirical S-N curves.

Table 5.1: Constants for SN100C-Cu fatigue equation (simple data fitting).

a	b	c	d
3.21×10^{7}	-1.47	1.3×10^{-4}	-2.7×10^{-6}

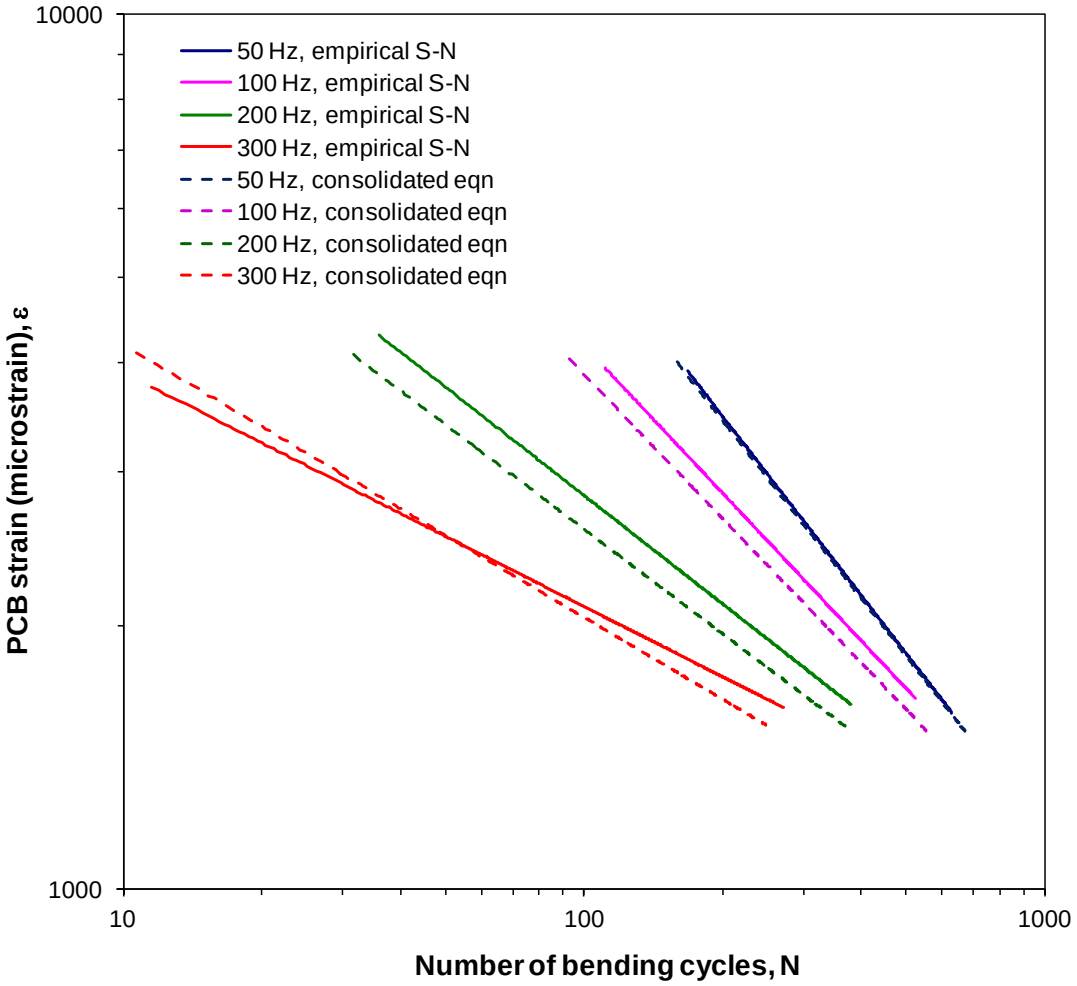


Figure 5.4: S-N curves from experimental data, plotted with S-N curves generated from consolidated equation.

5.3 Fatigue Model 2: Quantifying driving forces for fatigue

The discussions on frequency-dependent fatigue life in Chapter 4 suggest that embrittlement mechanisms at high strain rates are the cause of reduced fatigue life at higher frequencies. Evidence of embrittlement are fractures along IMC layers, and transgranular fractures across bulk solder grains that shorten the crack path. It is hypothesized that fractures along IMC layers occur because of the high stresses that develop in the solder as a result of elevated strain rates. Stress-strain curves for solder obtained from drop compression tests [36] show a markedly increased flow stress at high strain rates, compared to the stress at quasi-static loading rates. At

sufficiently high strain rates, the stresses which develop within the joint may exceed the IMC bond strengths. Because bulk solder cracks propagate adjacent to the copper pad, the region around the crack tip, where the strains (and strain rates) are elevated, can envelop IMC zones and promote overstress failures of IMC bonds. High strain rates also generally reduce the ductility and toughness of materials. This rate sensitivity may explain why bulk solder cracks (although they display considerably more ductile characteristics than IMC fractures) and can exhibit different degrees of brittleness and crack path variations at different bending frequencies. In order to capture embrittlement phenomena in a fatigue model, it is proposed that the common driver of the phenomena, which is strain rate $\dot{\varepsilon}$, be incorporated as a key parameter in the fatigue model.

The fatigue model developed in the previous section uses PCB strain as a parameter, and is therefore dependent on the geometry of the particular test vehicle used. A more universally applicable fatigue model is one which is independent of specimen geometry and can therefore be used by designers to estimate the fatigue life of solder joints in any board assembly design. To eliminate specimen geometry dependence, the PCB strains used as a loading parameter in the fatigue model may be converted to stress- or strain-based quantities at the solder joint level. For the fatigue model developed in this section, the PCB strains are converted to strains in the solder joint, using a shell-and-beam FEA model (Section 5.4). The strain ε_s at the edge of an intact solder joint (without cracks) is also proposed as a key loading parameter in the fatigue model. Each microstrain of PCB bending produces approximately 5μ of elastic strain at the joint edge, where loading is most severe. An implicit assumption in the S-N approach to fatigue failure modeling is that the

loading parameter does not change with crack growth. It should be noted that in reality, cracks initiate in the first few fatigue cycles of impact-induced loading, which would render a fatigue model based on intact joint strains physically meaningless; in addition, crack tip strains are orders of magnitudes higher than ε_s and also change dynamically with crack growth. Therefore, ε_s is simply a representation of the actual driving forces that propagate the crack, namely the plastic strains or stresses at the crack tip.

A purely empirical "embrittlement function" *B* is defined to capture the effects of strain rate $\dot{\varepsilon}$ and strain amplitude ε_s on the crack driving force. The simplest form of *B* is a product of the two parameters, defined by:

$$B = \dot{\varepsilon}\varepsilon_s = \omega{\varepsilon_s}^2 = 2\pi f(k\varepsilon)^2 \tag{5.3}$$

where $\dot{\varepsilon} = \varepsilon_s\omega$ is the sinusoidal strain rate magnitude, ω the angular frequency, and *k* the ratio between solder strain ε_s and PCB strain magnitude ε.

Equation (5.3) is used to evaluate *B* for the different combinations of frequency and strain in the S-N data previously obtained. Figure 5.5(a) is a plot of fatigue life *N* against *B*, while Fig. 5.5(b) depicts the original S-N data in the form of *N* against ε. By comparing the two plots, it can be seen that use of the embrittlement function collapses the separate S-N curves into a single B-N power law curve. The different S-N datasets, from which *B* values were evaluated, are shown as coloured lines in Fig. 5.5(a). The dashed line shows the global fit to the entire B-N dataset.

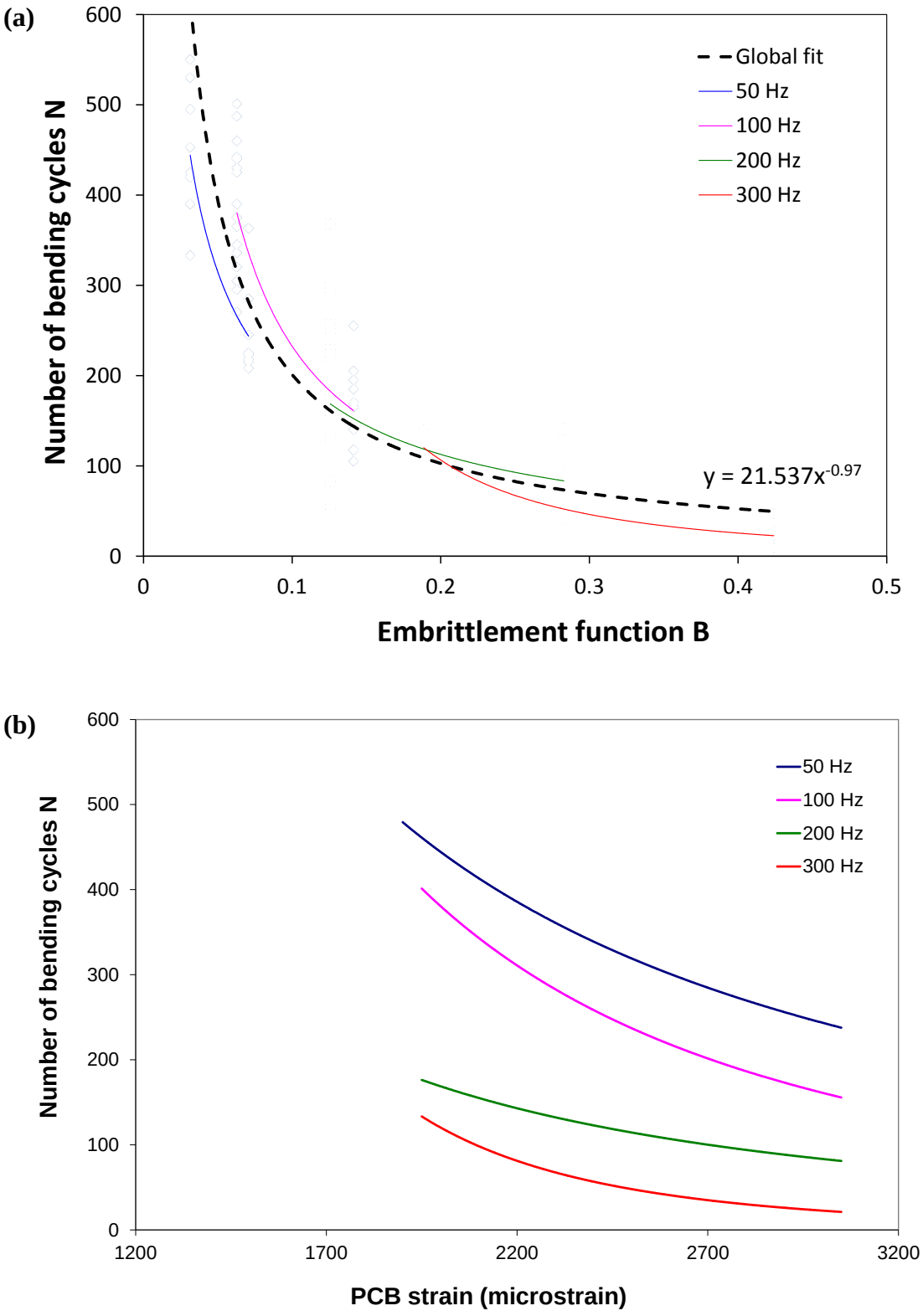


Figure 5.5: (a) Fatigue life vs B. (b) Fatigue life vs PCB strain.

The fatigue data can therefore be consolidated into a single elegant equation, described by

$$N = aB^b \tag{5.4}$$

where a and b are the power law constants for the B-N curve. The constants for SN100C-Cu joints are shown in Table 5.2.

Table 5.2: Constants for SN100C-Cu fatigue data expressed as a single B-N curve.

a	b
21.5	-0.97

5.4 Corrections for asymmetric bending

The fatigue data used in the development of the fatigue models were obtained from four-point bending tests, where the deflections along the PCB are symmetric about the center of the component. In a realistic system-level drop test, such a symmetric bending state is not guaranteed, and strains on either side of the component may differ. A study of the effect of asymmetric bending on solder joint loads is performed using computational modeling. Figure 5.6 shows examples of the cases modeled, ranging from a symmetric configuration at the top, to an anti-symmetric configuration at the bottom. Shell and beam elements were used to model the PCB/component and solder joints respectively. A model of the bend test modeled in ABAQUS v 6.8 is shown in Fig. 5.7(a). A shell-and-beam model has advantages over solid element models because it avoids stress singularities in solid elements at infinitely sharp corners, and precludes the need for modeling detailed fillet geometries to prevent instances of stress singularities. An example of a solid

element model composed of brick or hexahedral structural elements (C3D20) is shown in Fig. 5.7(b), while Fig 5.7(c) depicts an equivalent shell-and-beam model composed of S8R shell and B32 beam elements. Table 5.3 lists the parameters used for the numerical models; these values are representative, because the study is aimed at investigating trends rather than yielding actual values. For all the cases modeled, the PCB strain at one edge of the component is kept constant, while the strain at the other edge is varied.

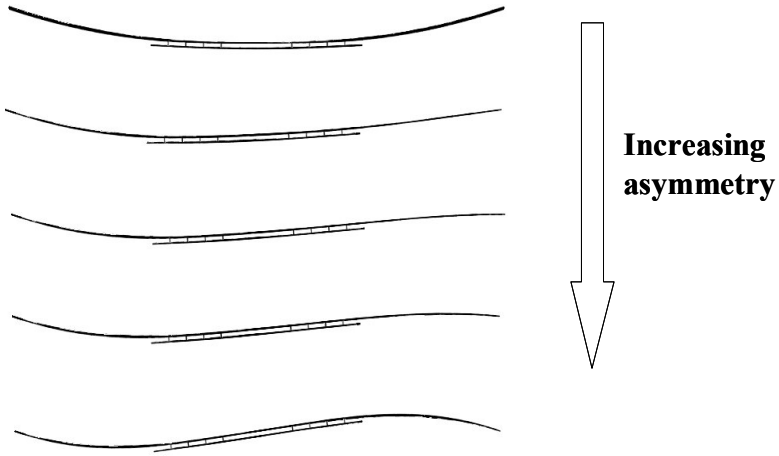


Figure 5.6: Asymmetric cases modeled (shell-and-beam FE models)

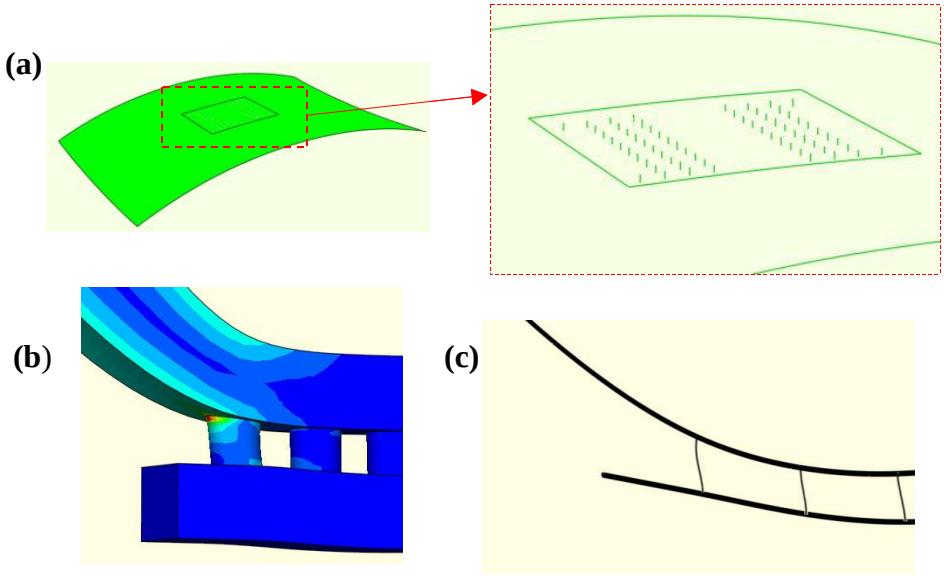


Figure 5.7: (a) Shell-and-beam FE model. (b) Magnified view of solid element model showing solder joints modeled as cylinders. (c) Magnified view of equivalent shell-and-beam model.

Table 5.3: Parameters used for FE shell-and-beam model.

Parameter	**Value**
E_{PCB}	14 GPa
E_{solder}	40 GPa
PCB thickness	0.8 mm
Package thickness	0.8 mm
Package size	12 x 12 mm
Pitch	1 mm
Joint height	0.3 mm
Joint diameter	0.28 mm

Figure 5.8 shows the results derived from computational modeling; they are plotted as solder strains (normalized to strains of a symmetric case) against bending asymmetry (quantified as the ratio between the PCB strains at opposite sides of the component). The degree of asymmetry ranges from -1, indicating antisymmetric bending, to 1, indicating symmetric bending. Solder joint strains decrease linearly with increasing asymmetry. In addition, the solder joints at the edge with low (or negative) PCB strains experience smaller loads. It is therefore important to determine the state of PCB flexure in the vicinity of the component before an assessment of the solder joint load can be made. If asymmetry exists, corrections can be applied to PCB strains before they are used in the fatigue model. It should be noted that these corrections are necessary because PCB strains are used as a parameter in the fatigue model. If the fatigue model were based on solder joint

strains, calculated by numerical or analytical models, then these corrections would not be required.

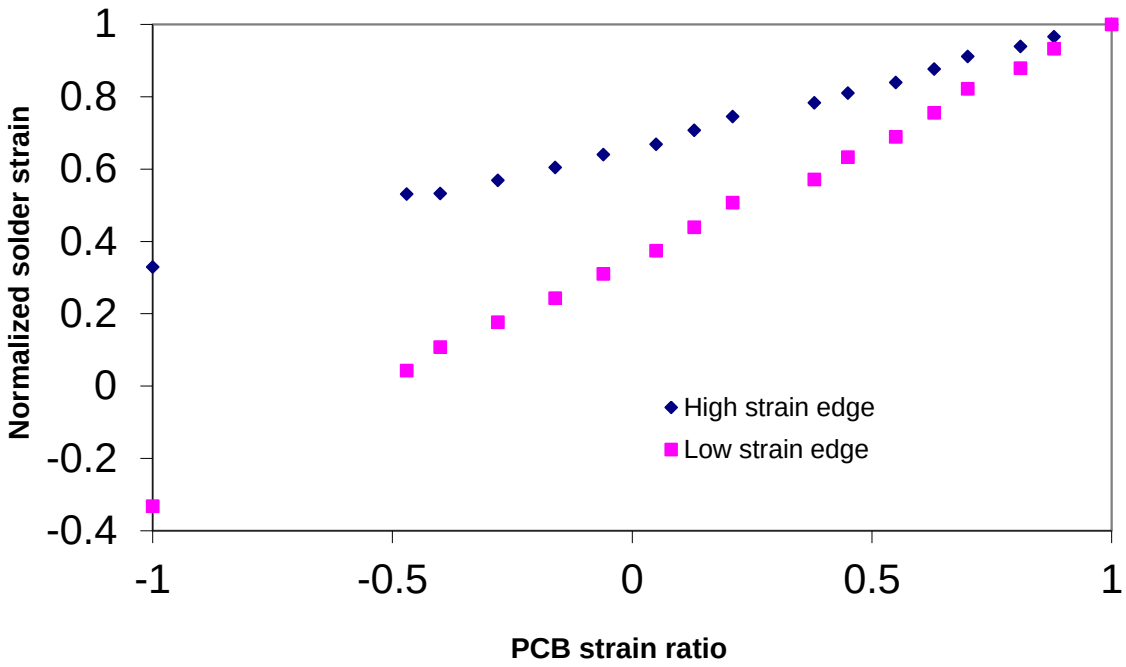


Figure 5.8: FE modeling results showing a reduction in solder joint load with bending asymmetry.

5.5 Validation of fatigue modeling methodology

Five types of experiments were performed to validate the fatigue modeling methodology:

1) Experiment 1: Edge impact (100 Hz)
2) Experiment 2: Edge impact (500 Hz)
3) Experiment 3: Variable frequency (35 Hz & 185 Hz)
4) Experiment 4: Nokia 2630
5) Experiment 5: Nokia 3110c

In each of these experiments, the test vehicle is subjected to loading conditions that are significantly different from the four-point bending used to generate the fatigue models. Estimates of damage caused by the load histories of the experiments are calculated using the Palmgren-Miner rule. The constant amplitude lives N_i for calculating damage sums/parameters are obtained from the two previously developed fatigue models. A damage sum that is close to unity validates the applicability of the fatigue model and life prediction methodology.

Experiment 1: Edge impact (100 Hz)

This experiment involves edge impacts on PCB assemblies to excite their vibration modes. The PCB was trimmed to a length which yields a free beam vibration frequency of 100 Hz. Figure 5.9 shows the test setup, while Fig 5.10 shows the PCB strains generated by impact. Despite dynamic flexure being initiated by impact at one end of the PCB, bending is symmetric because the flexural wave propagation is rapid enough for roughly equal strains to develop almost simultaneously at opposite sides of the component; there is only a very small phase difference between the Strain 1 and Strain 2 waveforms.

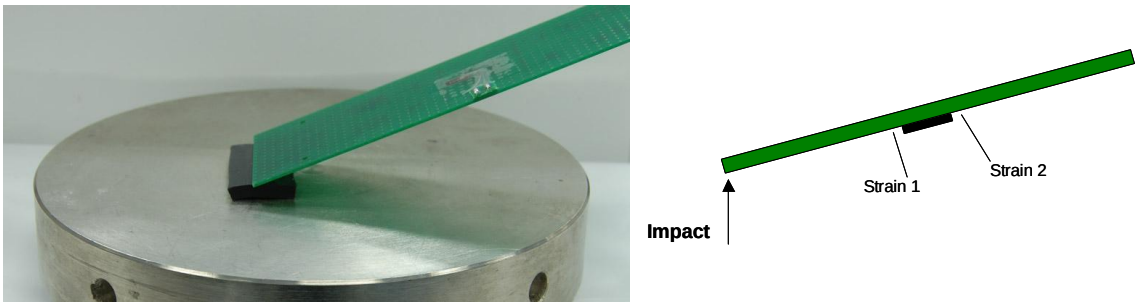


Figure 5.9: Test setup for Experiment 1: Edge impact experiments (100 Hz)

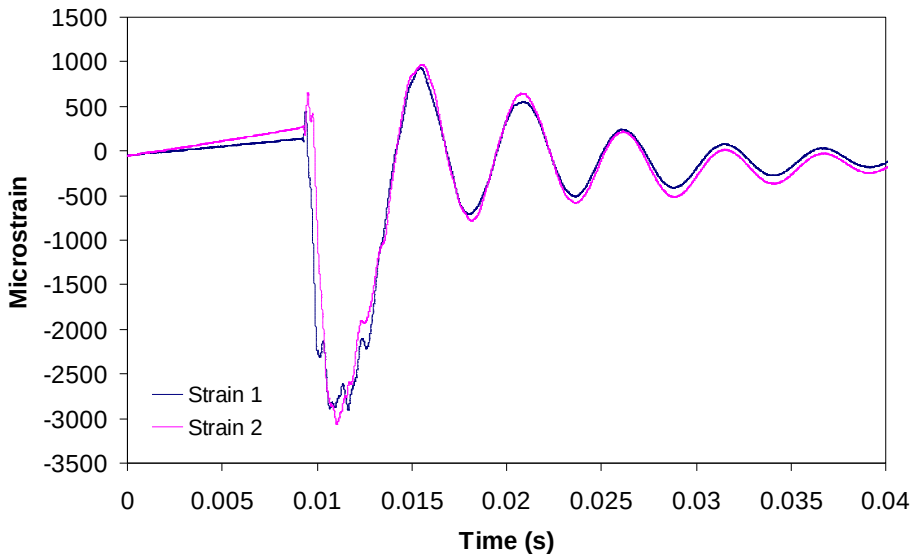


Figure 5.10: Strain waveforms from Experiment 1.

For Experiment 1, the load history is dominated by a single waveform of 3000μ amplitude and 100 Hz frequency. Tables 5.4 and 5.5 show the components of the damage parameter evaluated using Fatigue Models 1 and 2 respectively; the damage sums are close to unity for both cases.

Table 5.4: Damage parameter components and sums for Experiment 1 (using Fatigue Model 1).

Solder joint	Constant amplitude life N_1 (ε_1=3000u)	Number of cycles n_1 (3000u)	D
1	163	208	**1.28**
2	163	112	**0.69**
3	163	193	**1.18**
4	163	186	**1.14**

Table 5.5: Damage parameter components and sums for Experiment 1 (using Fatigue Model 2).

Solder joint	Constant amplitude life N_1 (ε_1=3000u)	Number of cycles n_1 (3000u)	D
1	143	208	**1.45**
2	143	112	**0.78**
3	143	193	**1.35**
4	143	186	**1.30**

Experiment 2: Edge impact (500Hz)

In order to produce higher bending frequencies, the test vehicle was mounted onto a stiff aluminium plate. The experimental setup is shown in Fig. 5.11. The plate was subjected to an edge impact that causes the entire structure to vibrate at a frequency higher than if the PCB itself were impacted (as in Experiment 1). The plate plays a role similar to that of a mobile phone casing in creating a stiffened assembly.

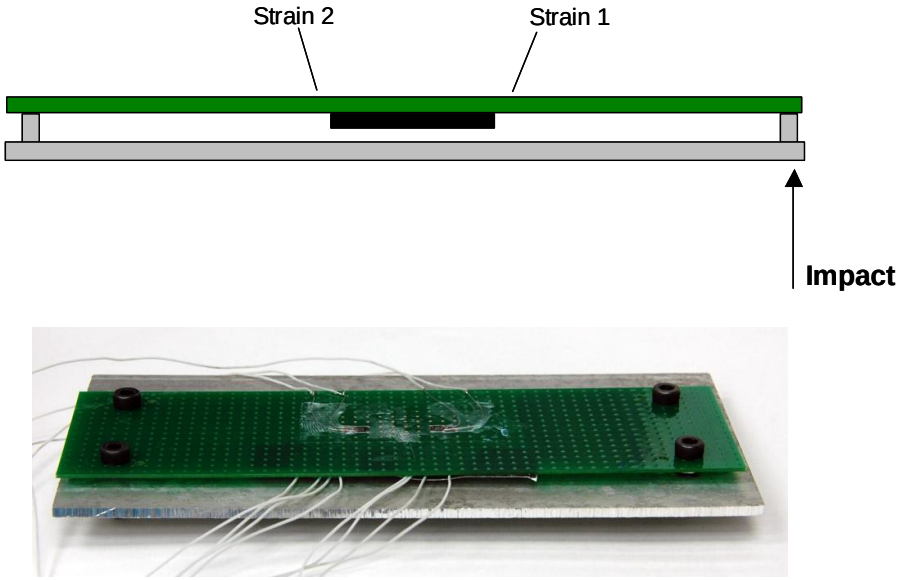


Figure 5.11: Test setup for Experiment 2: Edge impact (500 Hz).

Figure 5.12(a) shows measured PCB strains at opposite sides of the component during an impact test. A magnified view of the strain waveform corresponding to the first bending cycles is shown in Fig. 5.12(b). The strain waveforms are observed to be composed of several frequency components. Figures 5.12(c) and (d) show the frequency components, deduced from observation, which constitute the waveforms in Fig. 5.12(b). These waveforms are concluded to be composed of several modes, which are 1) a symmetric 500 Hz mode; 2) an anti-symmetric 1100 Hz mode; and 3) an anti-symmetric 4800 Hz mode. Owing to the small amplitudes and anti-symmetric bending of the high frequency modes, only the symmetric 500 Hz mode is considered in calculating the damage parameter. Tables 5.6 and 5.7 show the damage parameters evaluated using Fatigue Models 1 and 2 respectively. The damage parameter values are close to unity for Fatigue Model 2, but Fatigue Model 1 underestimates slightly the fatigue life in these experiments.

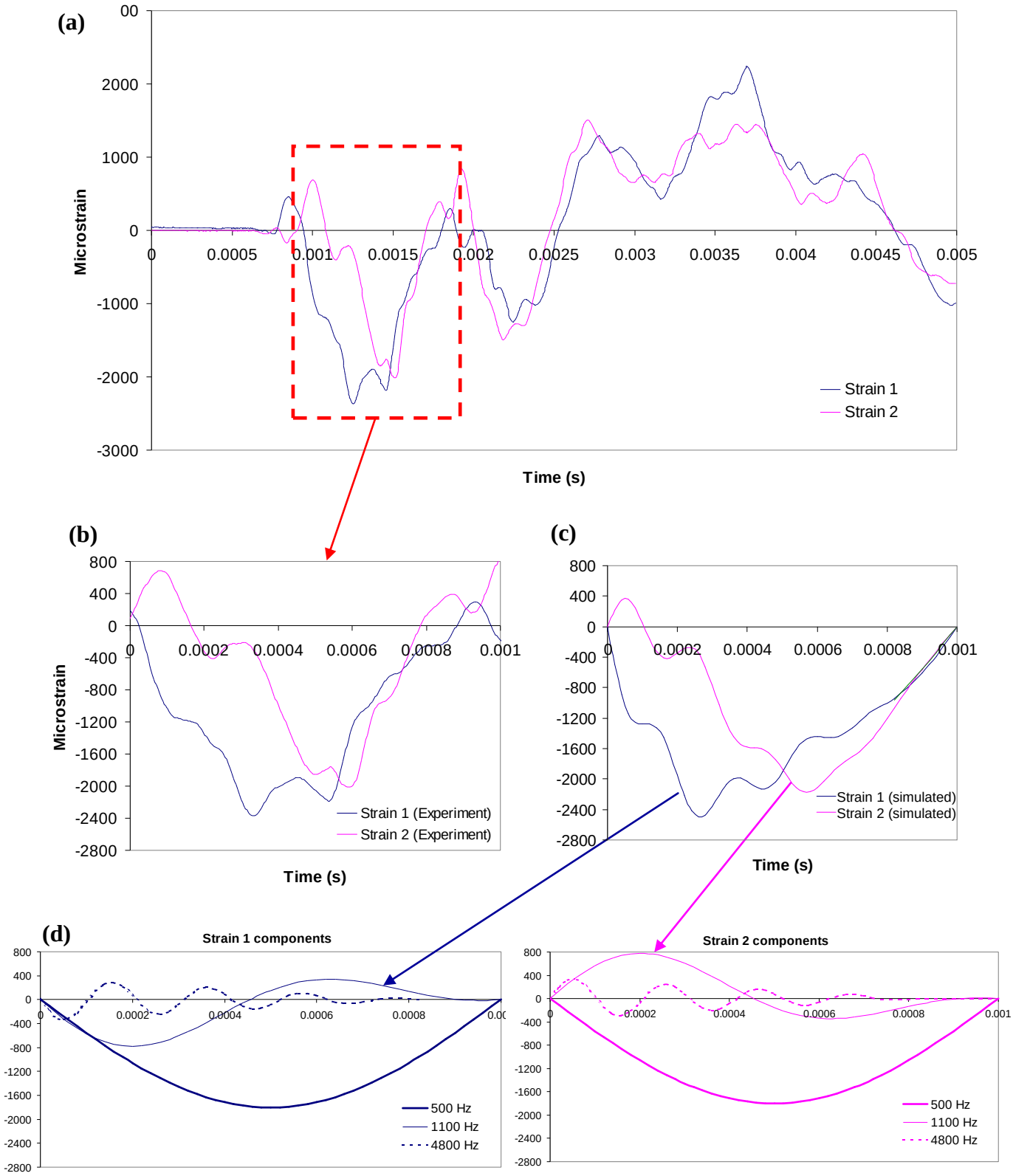


Figure 5.12: (a) Strain waveforms for Experiment 2. (b) Magnified view of first pulse. (c) Deduced first pulse components. (d) Frequency components of deduced pulses.

Table 5.6: Damage parameter components and sums for Experiment 2 (using Fatigue Model 1).

Solder joint	**N_1 (ε_1=2000u)**	**N_2 (ε_2=1800u)**	**N_3 (ε_3=1000u)**	**N_4 (ε_4=900u)**	**n_1 (2000u)**	**n_2 (1800u)**	**n_3 (1000u)**	**n_4 (900u)**	**D**
1	39	58	368	485	9	30	9	30	**0.83**
2	39	58	368	485	18	53	18	53	**1.53**
3	39	58	368	485	19	53	19	53	**1.55**

Table 5.7: Damage parameter components and sums for Experiment 2 (using Fatigue Model 2).

Solder joint	**N_1 (ε_1=2000u)**	**N_2 (ε_2=1800u)**	**N_3 (ε_3=1000u)**	**N_4 (ε_4=900u)**	**n_1 (2000u)**	**n_2 (1800u)**	**n_3 (1000u)**	**n_4 (900u)**	**D**
1	66	81	254	311	9	30	9	30	**0.64**
2	66	81	254	311	18	53	18	53	**1.17**
3	66	81	254	311	19	53	19	53	**1.19**

Experiment 3: Variable frequency (35 Hz & 185 Hz)

In this experiment, a load history of variable frequency was generated. The boards were impacted along an edge, as in Experiment 1, but have a shorter span in order to yield a higher vibration frequency of 185 Hz. To generate a low frequency, a mass is attached to the end of the board opposite the impact point; this enables a low frequency of 35 Hz to be generated. The test setup and corresponding waveforms produced are shown in Fig. 5.13. The load history consists of alternating blocks of 185 Hz and 35 Hz pulses, each lasting for approximately 10% of the constant amplitude fatigue life. Corrections to the PCB strain are made for the significantly asymmetric bending at 35 Hz. Tables 5.8 and 5.9 show the damage parameter values calculated using Fatigue Models 1 and 2 respectively. The damage parameter values are close to unity for both cases.

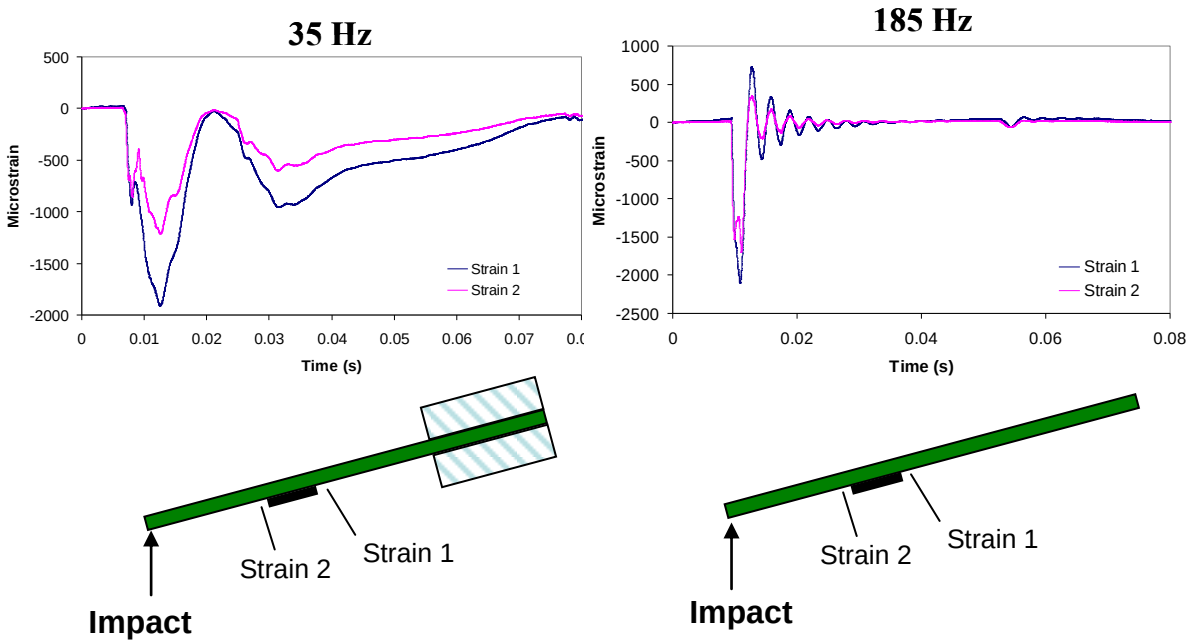


Figure 5.13: Test setup for Experiment 3: Variable frequency.

Table 5.8: Damage parameter components and sums for Experiment 3 (using Fatigue Model 1).

Solder joint	**N_1 (f_1=185Hz)**	**N_2 (f_2=35Hz)**	**n_1 (185Hz)**	**n_2 (35Hz)**	**D**
1	270 (ε_1=1800u)	607 (ε_2=1700u)	120	209	0.79
2	346 (ε_1=1600u)	1502 (ε_2=900u)	181	400	0.79
3	270 (ε_1=1800u)	607 (ε_2=1700u)	160	389	1.23
4	346 (ε_1=1600u)	1502 (ε_2=900u)	200	492	0.91

Table 5.9: Damage parameter components and sums for Experiment 3 (using Fatigue Model 2).

Solder joint	**N_1 (f_1=185Hz)**	**N_2 (f_2=35Hz)**	**n_1 (185Hz)**	**n_2 (35Hz)**	**D**
1	213 (ε_1=1800u)	1195 (ε_2=1700u)	120	209	**0.74**
2	267 (ε_1=1600u)	4104 (ε_2=900u)	181	400	**0.77**
3	213 (ε_1=1800u)	1195 (ε_2=1700u)	160	389	**1.08**
4	267 (ε_1=1600u)	4104 (ε_2=900u)	200	492	**0.87**

Experiment 4: Nokia 2630

In this experiment, the test vehicle is mounted within a mobile phone casing in order to produce load histories similar to that seen in system level tests. Figure 5.14 shows the test setup, with strain gauges mounted on the PCB at each edge of the component. The location of the component simulates the location of an area array package on an actual product board assembly. Impact is applied at the end of the casing as indicated in Fig. 5.14. Figure 5.15 shows the strain waveforms generated during impact. The difference in the magnitudes of Strains 1 and 3 (along the long dimension of the board) indicate that bending is asymmetric, owing to the location of Strain gauge 1 near the edge of the PCB. The waveforms are dominated by a single frequency, estimated to be 660 Hz. It should be noted that significant transverse strains are present, as indicated by Strains 2 and 4. However, only Strains 1 and 3 are used to estimate damage.

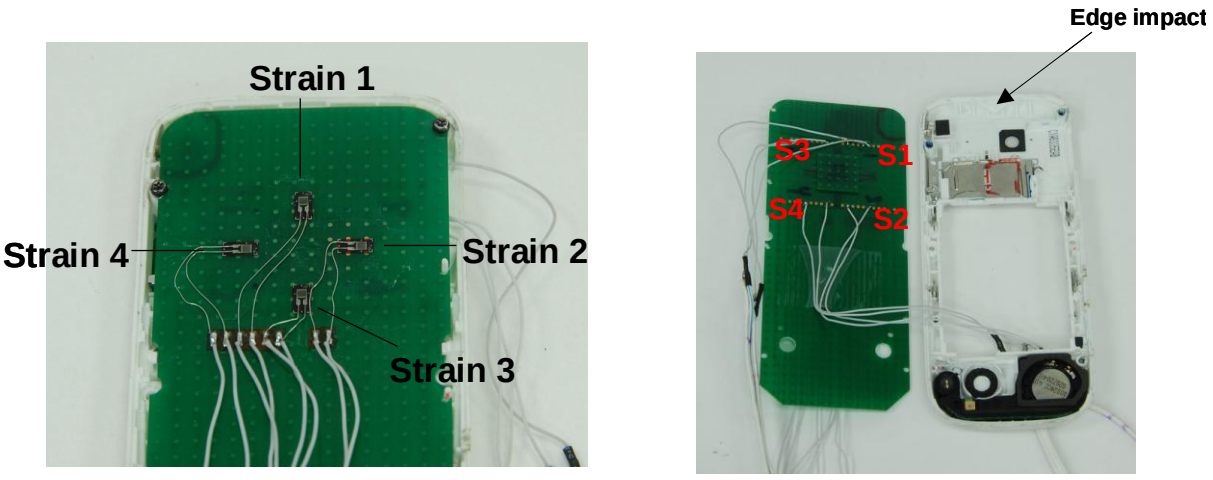


Figure 5.14: Test setup for Experiment 4: Nokia 2630.

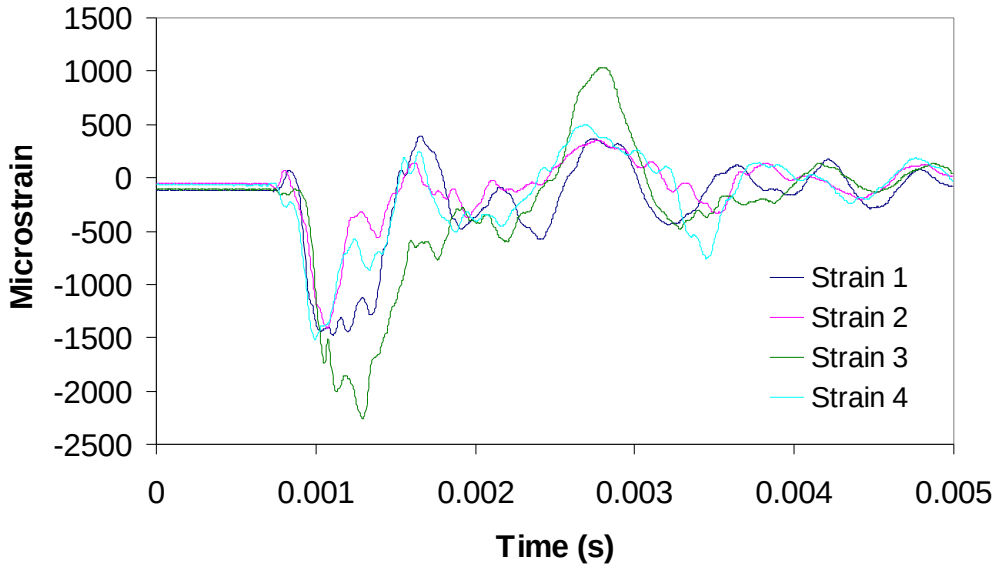


Figure 5.15: Strain waveforms from Experiment 3.

Tables 5.10 and 5.11 show the damage parameter components and sums for Fatigue Models 1 and 2 respectively. Only the first impact pulse is used for damage calculations. The bending frequency is taken to be 660 Hz, and the strain amplitudes are estimated from the peaks of Strains 1 and 3. Because of the variability in loading over multiple impacts, the measured strains were observed cover a wide range; for example, Strain 3 values range from 1200μ to 2200μ. In order to perform damage calculations, measurements were categorised or "binned" into three discrete levels, namely 1400μ (representing a range of 1200μ to 1550μ), 1700μ (representing a range of 1550μ to 1850μ), and 2000μ (representing a range of 1850μ to 2200μ). Corrections were applied to the strains to account for asymmetry in bending. The corrected strains used in the fatigue models are shown in parentheses in the damage parameter sum tables.

Table 5.10: Damage parameters components and sums for Experiment 4 (using Fatigue Model 1).

Solder joint	**N_1 (2000u)**	**N_2 (1700u)**	**N_3 (1400u)**	**n_1**	**n_2**	**n_3**	**D**
1	27 (ε_1=1800u)	51 (ε_2=1550u)	114 (ε_3=1250u)	16	8	1	**0.76**
2	44 (ε_1=1600u)	86 (ε_2=1350u)	176 (ε_3=1100u)	22	10	1	**0.62**
3	27 (ε_1=1800u)	51 (ε_2=1550u)	114 (ε_3=1250u)	32	26	20	**1.88**
4	44 (ε_1=1600u)	86 (ε_2=1350u)	176 (ε_3=1100u)	40	44	68	**1.80**

Table 5.11: Damage parameter components and sums for Experiment 4 (using Fatigue Model 2).

Solder joint	**N_1 (2000u)**	**N_2 (1700u)**	**N_3 (1400u)**	**n_1**	**n_2**	**n_3**	**D**
1	62 (ε_1=1800u)	82 (ε_2=1550u)	125 (ε_3=1250u)	16	8	1	**0.36**
2	78 (ε_1=1600u)	108 (ε_2=1350u)	161 (ε_3=1100u)	22	10	1	**0.38**
3	62 (ε_1=1800u)	82 (ε_2=1550u)	125 (ε_3=1250u)	32	26	20	**0.99**
4	78 (ε_1=1600u)	108 (ε_2=1350u)	161 (ε_3=1100u)	40	44	68	**1.34**

There is a wide difference in the damage parameter sums calculated using the two models. The reason for the difference is that the 660 Hz frequency requires the fatigue models to be extrapolated beyond the ranges used to fit the models. Fatigue Model 2 tends to overestimate the fatigue life at high frequencies (or high B). There are also significant deviations in the damage sums from unity. This difference is attributed to the effects of transverse strains, which were not considered in the damage calculations. On average, the damage parameter sums remain close to unity, but safety factors should be used when applying the fatigue models in their current form to a system level board.

Experiment 5: Nokia 3110c

In this experiment, the test vehicle is mounted in another mobile phone casing with the component located at a central position on the board, in contrast to the edge location in Experiment 4. Figure 5.16 shows the test setup and PCB strains. The bending frequency and amplitude of the dominant vibration mode are approximately 700 Hz and 1300μ respectively. Tables 5.12 and 5.13 show the damage parameter sums calculated using Fatigue Models 1 and 2 respectively. Both models tend to underestimate the fatigue life.

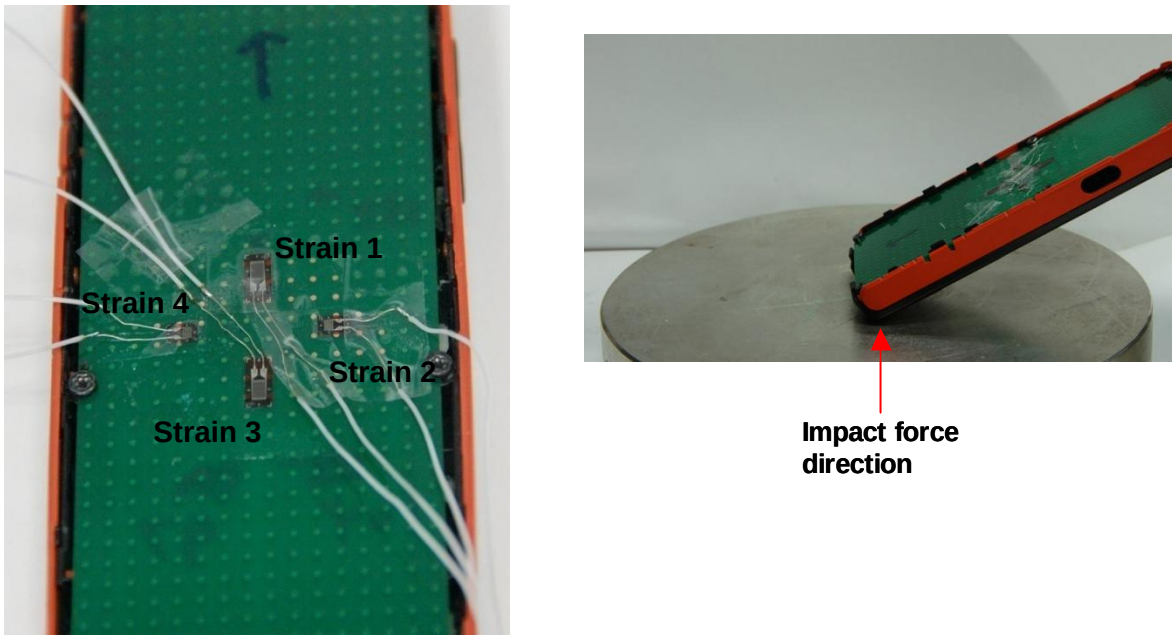


Figure 5.16: Test setup for Experiment 4: Nokia 3110c.

Table 5.12: Damage parameter components and sums for Experiment 5 (using Fatigue Model 1).

Solder joint	**N_1 (1300u)**	**n_1**	**D**
1	86 (ε_1=1300u)	104	**1.21**
2	86 (ε_1=1300u)	164	**1.91**
3	86 (ε_1=1300u)	188	**2.19**
4	86 (ε_1=1300u)	97	**1.13**

Table 5.13: Damage parameter components and sums for Experiment 5 (using Fatigue Model 2).

Solder joint	**N_1 (1300u)**	**n_1**	**D**
1	110 (ε_1=1300u)	104	**0.95**
2	110 (ε_1=1300u)	164	**1.49**
3	110 (ε_1=1300u)	188	**1.71**
4	110 (ε_1=1300u)	97	**0.88**

5.6 Summary and conclusions

This chapter has presented two fatigue life models and a methodology for estimating the fatigue life of solder joints under dynamic PCB bending. The fatigue models essentially consolidate the experimental data into simplified models for estimating the constant amplitude/frequency fatigue life. The first fatigue model is based on basic curve fitting to S-N data. The second model is founded on parameters that are viewed as drivers of brittle fatigue fracture, namely strain rate and strain amplitude; these parameters are used in a proposed "embrittlement function" that is shown to follow a simple power law relationship with fatigue life. In the case of variable amplitudes and/or frequencies, the Palmgren-Miner rule is used to sum up the damage contributions of the constituent components of variable load histories. Any influence of load sequence on fatigue life is ignored. Use of the fatigue models and damage rule has to be accompanied by an accurate decomposition of complex load histories into their constituent frequency components and load amplitude levels.

Validation experiments show that the fatigue models and proposed methodology yield a reasonably good prediction of fatigue life in cases where bending occurs predominantly along the long axis of the board. Despite being based on a limited set of data, the fatigue models are able to provide fairly accurate damage estimates for frequencies well beyond the data range used to fit the models. However, as the models are formulated using data from single-plane bending tests, significant deviations in the Miner Sums from unity are observed in cases where flexure in more than one plane occurs, for example in Experiments 4 and 5, where transverse strains are observed.

While PCB bending strains around the component are convenient to measure, and sufficient as an estimate of the boundary conditions, there are clear advantages to using solder joint strains or stresses as the load parameter in the fatigue models. Having information on actual solder joint loads will avoid the need to apply correction factors for asymmetric bending, and can provide more accurate damage estimates in cases of multi-plane bending. Solder joint loads may be estimated using numerical or analytical techniques. For example, computational modeling of the mobile device at the design stage can provide information on solder joint loads, which can then be input into a fatigue life model to determine the robustness of the design.

Chapter 6

Conclusions and Recommendations

This research has been motivated by the desire to address a poorly-understood reliability issue for electronic assemblies, which is the failure of solder joints under dynamic loads associated with drop impact. This reliability problem came to the forefront several years ago, when manufacturers of electronic assemblies encountered solder joint failures caused by drop impacts of mobile devices. The issue has been compounded by several factors, namely the increased use of mobile devices, the switch from lead-based solders to lead-free solders, and the fact that high strain rates exacerbate the failure of solder joints. Solder joint failure under drop impact is a key reliability issue that has to be resolved by manufacturers of portable electronics, in addition to thermal cycling fatigue issues.

Today's industry solution, for ensuring that components and their solder joints survive drop impacts, is to apply underfill adhesive that fills the spaces between solder joints. In essence, this solution bonds the entire component to the PCB, and limits the stresses and deformation developed in solder joints. However, the underfilling process entails additional steps to manufacture, and also increases the difficulty of reworking or replacing components. Underfilling is conventionally used for preventing thermal cycling fatigue in fine pitch solder joints, but has become the main solution for preventing joint failures caused by drop impact. With a better understanding of drop impact failure, designers and engineers of mobile electronic devices can determine whether an underfill process is needed, or how to design their devices to avoid the need for underfilling.

A key reason for the limited understanding of the drop impact problem is the lack of effective test methods for characterising failure. The standard drop test method prescribes a specific load history to the solder joints, which is very different from actual load histories encountered in the field. While some excellent alternative test methods have been proposed, these are also limited in their ability to characterise failure for a wide range of conditions.

Life prediction methodologies for complex load histories, such as those encountered in drop impact, typically involve the use of fatigue S-N data and a cumulative damage law to estimate damage. However, these methodologies have not been validated with respect to variable load histories that typically occur in drop impact.

6.1 Contributions to the State of Knowledge

1) An insight into damage development in solder joints under drop impact

The first contribution of this research is identification of the nature of fatigue damage in solder joints when a mobile device experiences a series of drops. In-situ monitoring of crack growth in solder joints during product drop tests provides an insight into the chain of events linking impact forces applied to the external casing of a mobile device to the failure of solder joints on the internal board assembly. Results show a definitive link between failure modes and crack growth rates, where previously such a link could only be hypothesised. Solder joint failure in a typical drop impact occurs via extremely low cycle fatigue, with virtually no crack initiation phase.

2) A fundamental understanding of very low cycle fatigue of solder joints

The second contribution of the research undertaken is a comprehensive characteristisation of fatigue in solder joints for very low cycle fatigue. Studies were performed to determine the influence of various parameters – materials, load frequency, load amplitude, temperature and fatigue load sequence – on the fatigue life of solder joints under dynamic PCB bending. The fatigue life was found to be highly dependent on the bending frequency, whereby higher frequencies promote brittle failures and shorter fatigue lives. High strain amplitudes were also found to increase the occurrence of brittle failure modes. In general, variable load histories are slightly detrimental to fatigue life compared to uniform amplitude loading.

3) Development of novel and practical experimental methods

The design and implementation of an experimental method for tracking crack growth in a single solder joint during drop impact was accomplished. This tool enables investigations into how crack growth may be accelerated or retarded by specific microstructural features. A high speed cyclic bend test method for applying dynamic bending loads directly to PCB assemblies was refined and shown to be effective in the fatigue characterization studies. This enables investigation of the effects of various parameters and combinations of loading cycles on fatigue damage in solder joints.

4) Development and validation of a fatigue life prediction methodology

The research undertaken has also resulted in the development and validation of a life prediction methodology for solder joints under drop impact loads. Predictive

fatigue models were developed based on data obtained from dynamic bend tests, and damage is estimated using a simple cumulative damage model. Validation was obtained via several test cases which had variable load histories.

5) Papers published in this research

S.K.W. Seah, E.H. Wong, and V.P.W. Shim, "Fatigue crack propagation behavior of lead-free solder joints under high-strain-rate cyclic loading", 2008, Scripta Materialia [44].

S.K.W. Seah, and V.P.W. Shim, “Solder Joint Failure from Impact-induced PCB Flexure”, 2010, Proceedings of the 10th IMPLAST Conference [39].

E.H. Wong, S.K.W. Seah, and V.P.W. Shim, "A Review of Board-Level Solder Joints for Mobile Applications", 2008, Microelectronics Reliability [57].

Wang J., Seah S.K.W., Wong E.H., and Cadge D., "Fracture mechanics study of fatigue crack growth in solder joints under drop impact", 2008, Proceedings of the 58th Electronic Components and Technology Conference [58].

6.2 Recommendations for future work

1) Elimination of geometry dependence of fatigue models

The fatigue model developed in the present work is defined in terms of PCB strain and is therefore only directly applicable to a particular test vehicle design having particular solder joint and pad dimensions. Dependence on test vehicle design can be eliminated by translating PCB strains to solder joint strains/stresses through computational modeling, as is commonly performed in many modeling studies [47-50]. Alternatively, correction factors may be established – using computational or analytical modeling [39] – to account for differences in loading severity between different test vehicle geometries, for the same PCB strain. These suggested methods for adapting the fatigue model to cover a wider application are based on the assumption that variations in test vehicle geometry affect only the load amplitudes experienced by the solder joint, and not the fatigue damage process. Therefore, one suggestion for future work is to characterise the effect of the test vehicle geometry in order to verify this assumption. Another suggestion is to investigate the effects of solder ball and/or pad dimensions on crack growth patterns and fatigue life.

2) Understanding fatigue for plate bending conditions

The fatigue data generated in the present work was obtained from four-point bending tests, which are suited for a cost-effective and controlled study of fatigue characteristics. The damage modeling methodology provided good predictions because the validation tests were performed with bending predominantly in one plane. In actual applications, PCBs will experience complex modes of plate bending, with significant levels of transverse bending and twisting, as well as

complexities due to PCBs being attached to device housings that also flex. The most practical method to handle such complex bending states is to computationally model the dynamic board assembly deformations in order to estimate the resulting loads on solder joints. Another suggestion for future work is to validate fatigue models using variable load histories generated by a range of dynamic plate bending conditions. It would also be highly useful to study the effect of crack growth direction, because the crack growth directions in the present work were predominantly along the length of the test vehicle sample.

3) Further investigation of load sequence effects

An unusually high crack growth rate was observed immediately after a low-to-high cyclic load transition, which may account for resulting cumulative damage parameter values of less than unity for the majority of the variable sequences tested. While such a reduction in fatigue life is insignificant for practical applications, this phenomenon is interesting and warrants further study. In addition, the influence of the R ratio – the ratio of minimum to maximum peak strain of a fatigue cycle – on sequence effects, remains to be examined.

4) Controlling crack arrest and catastrophic crack growth

Significant scatter in the fatigue data was observed for certain solder alloys, especially for attachments to ENIG pads. The failure mode analysis employed indicates that bulk solder, brittle IMC or mixed mode failures are equally likely to occur for these material systems. There is much scope for work in developing deterministic methods to control failure under high strain rates for these materials.

A starting point is to understand the factors which cause a crack to move from the bulk solder into the IMC region, and vice versa.

5) Fatigue models based on a crack growth approach

The fatigue models in the current work do not take into account evolution of the crack tip driving force as a crack progresses. A crack growth model is much more physically accurate than an S-N curve model, although more complicated. An early relevant study was presented by Wang et al. [52] who performed computational simulations to evaluate the three-dimensional J-integral around the crack front in a solder joint. A suggestion for future work is to further develop this crack growth approach for modeling fatigue crack growth in solder joints.

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Appendix A

Test Specimen Design

Figure A.1 shows a schematic diagram of the test vehicle used, together with the solder pad layout and dimensions. The pad layout has two key differences from a standard area array layout:

1) There are offset corner joints at the edge of the component that are monitored for failure. Modeling (Fig. A.3) shows that the corner joints experience approximately 20% higher stresses than if there were a full column of solder joints at the edge. This pad layout ensures that the earliest failures occur in a controlled manner in a few selected joints that constitute the focus of the experiment. If there were a full column of joints at the component edge, failure would occur at random joints along the entire column because all the joints in the column would experience similar levels of loading.

2) The central columns of joints are removed because most of the loading is sustained by the outer columns of solder joints. This is illustrated in Fig. A.2.

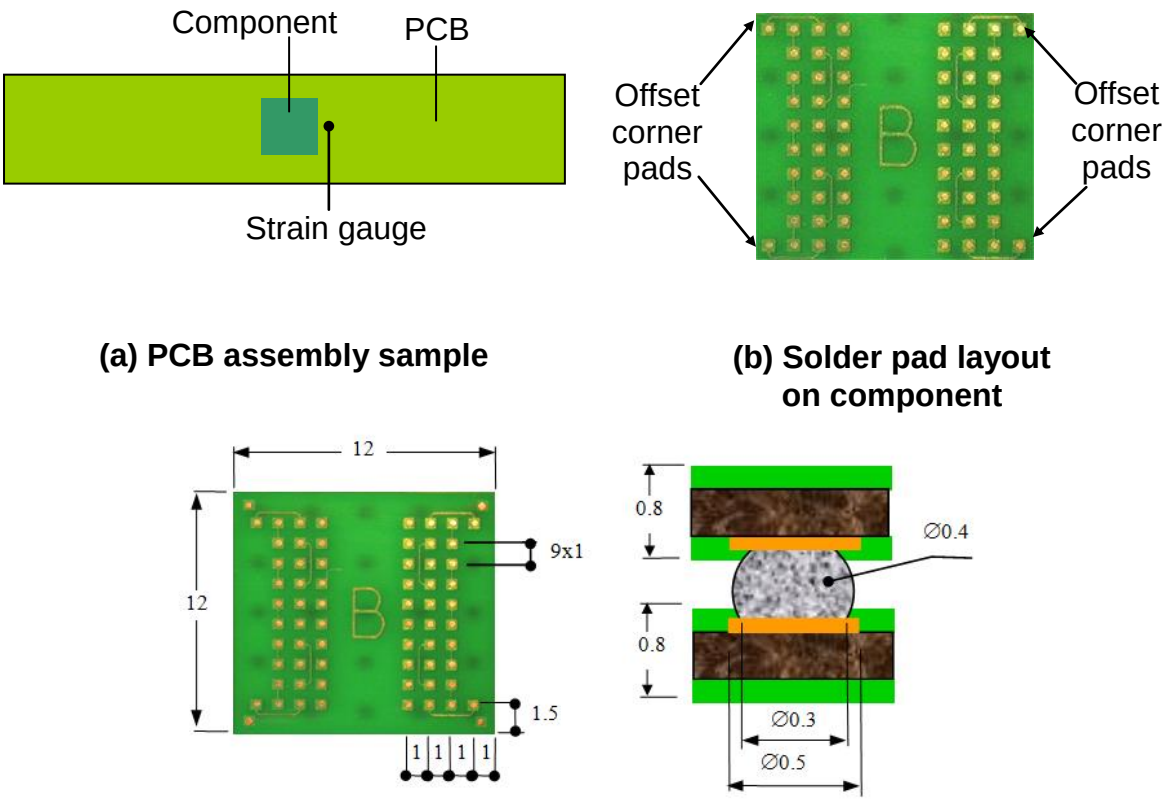


Figure A.1: Board assembly used for experiments; (a) Schematic diagram of PCB assembly bending sample; (b) Solder pad layout; and (c) Critical dimensions.

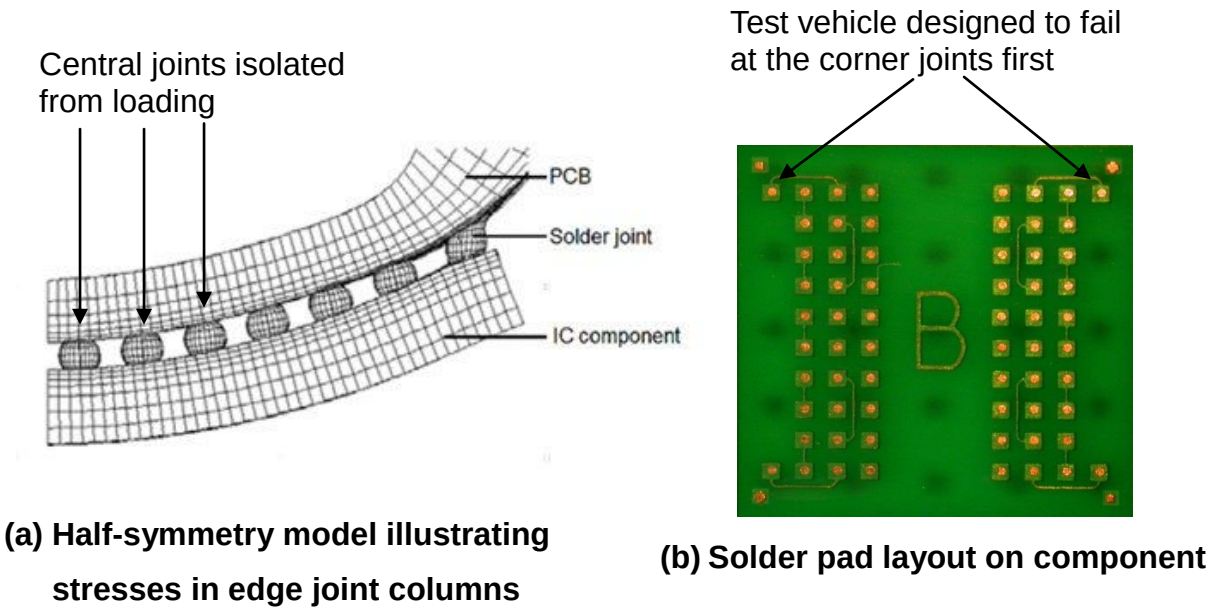


Figure A.2: Pad layout design is based on mechanics of loading on solder joints observed during PCB bending.

In addition, this pad layout provides failure data from four solder joints per test vehicle. This is deemed superior to the standard industry practice of daisy-chaining the entire array of solder joints. In a typical daisy-chained layout, the initial failure of *any* joint in the array is taken as the failure of the component.

Computational modeling was performed to investigate the effect of failure of any corner joint on the stresses carried by the other corner joints. The model, constructed in ABAQUS v6.8, is shown in Fig. A.3. The material properties and mesh details for this solid element model are the same as those provided for the FE study of Section 5.4. This study focuses on trends and relative changes in loads, rather than absolute levels of load in the solder joints. Figure A.4 shows the permutations of corner solder joint failure that were modeled. For all cases, the axial force (F_1), shear force (F_2) and σ_{11} of the upper left corner joint at the pad edge were monitored. Note that the axial direction 1 is along the axis of the solder joint, i.e. normal to the plane of the PCB and component, while direction 2 is along the length of the PCB.

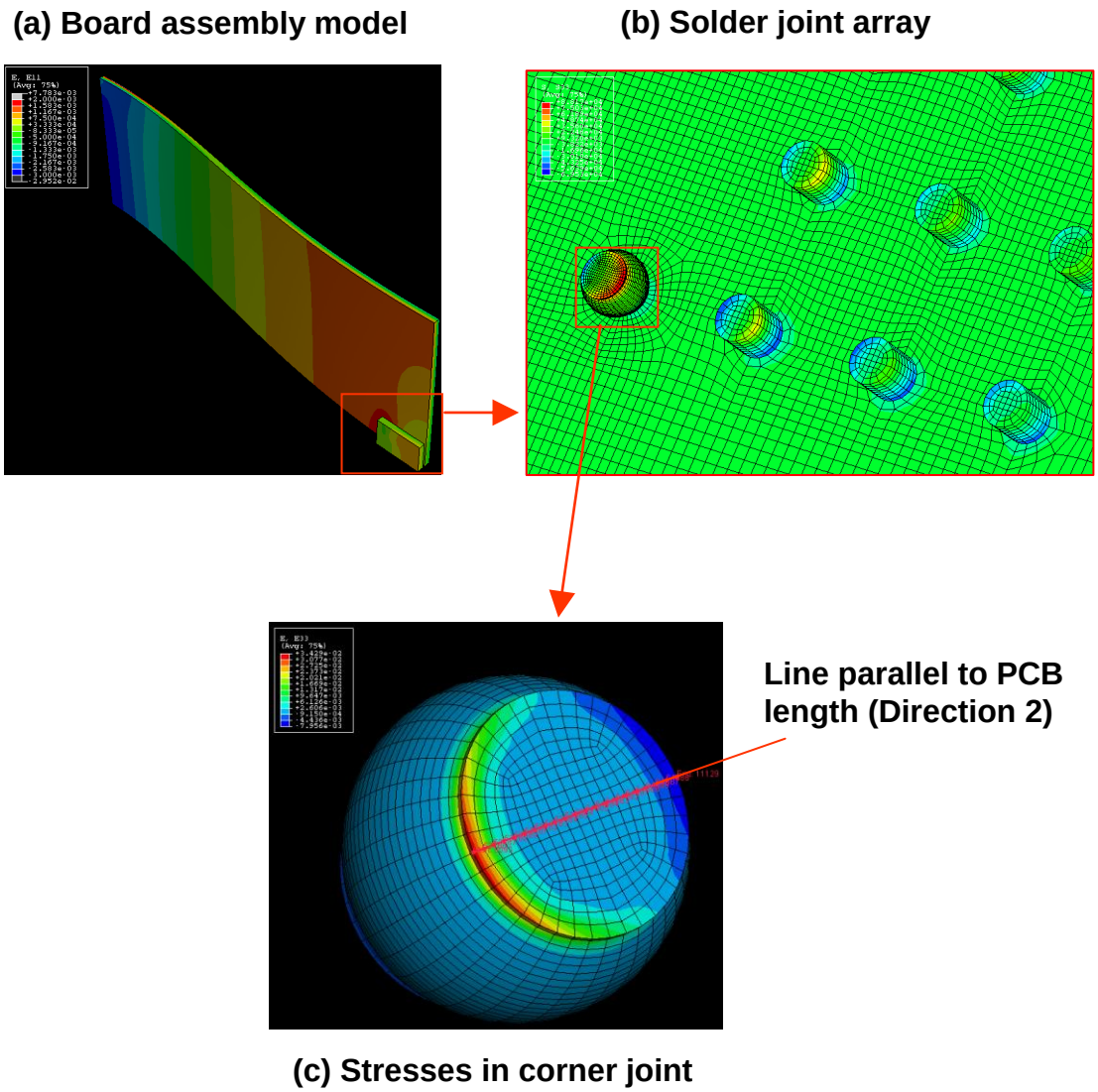


Figure A.3: FE model used to design the test vehicle.

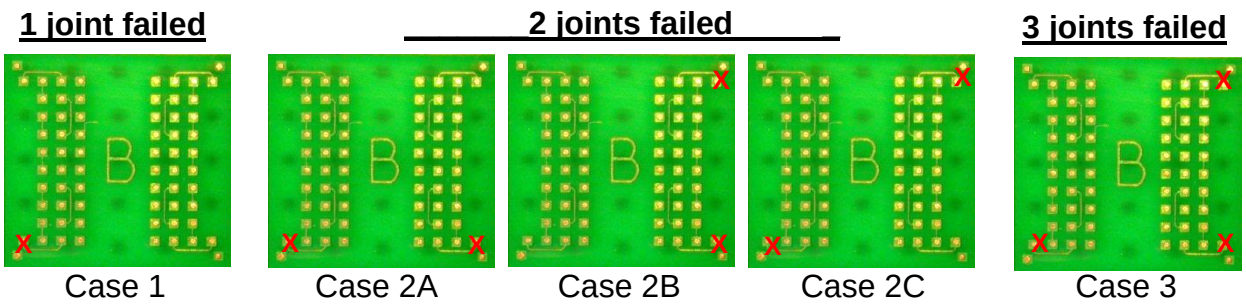


Figure A.4: Permutations of corner joint failure modeled to investigate their effect on stresses in the upper left corner joint.

Table A.1 shows changes in the loading on the upper left corner joint for the various cases of corner solder joint failure. The values are normalized with respect to a case where all corner joints are intact. The maximum change in loading is 3% for a case of three failed corner joints, which is acceptable, given that variations in material strength and manufacturing (e.g. fillet radius and pad dimensions) cause much larger changes in failure results.

Table A.1: Change in loading on upper left corner joint for various cases of corner joint failures (values are normalized with respect to a case of no corner joint failure).

	Case				
	1	**2A**	**2B**	**2C**	**3**
σ_{11}	1%	-2%	0	-1%	-1%
F_a	1%	-1%	0	0%	0
F_t	1%	-3%	0	-2%	-3%

In summary, the test vehicle for dynamic PCB bending was designed to ensure controlled failure in specific joints that are instrumented and monitored. Ensuring that failure occurs in the joints that are being observed is especially important in fatigue experiments, where large scatter in failure data is common. Four data points are obtainable from a single test vehicle. The four corner joints are sufficiently isolated from one another, such that failure of multiple corner joints will have minimal effect on loading of the remaining corner joints.

Appendix B

Background Information for Crack Growth Studies

B.1 Equipment specifications

Current source: Keithley 2410 Source Meter

Current source accuracy: 0.07% of current reading

Voltage measurement 1: HP 8.5-digit Digital Reference Multimeter

Accuracy: 4 μV

Resolution: 0.050 μV

Sampling rate: 1000 S/s

Voltage measurement 2: 16-bit oscilloscope (Yokogawa DL750)

Accuracy: 25 μV

Resolution: 0.42 μV

Sampling rate: 1 million S/s

B.2 Sources of error

Fluctuations in the measured voltage have been observed to be caused by the following factors:

1) Joule heating of the circuit.
2) Body heat due to handling (e.g. from fingers).
3) Environmental temperature fluctuations.

Errors were minimized and fluctuations stabilized by the following measures:

1) Set source current to 200 mA, which is a compromise between joule heating effects and measurement sensitivity for the circuit used.
2) Wait for the voltage to stabilize after any setup and/or handling procedures. Voltage stabilizes typically within 5 minutes of 200 mA current heating.
3) Set filter to 5 kHz to minimize measurement noise. Note that measurement noise far exceeds the accuracy and resolution limits of the equipment.

4) Tie down main signal cables to equipment to eliminate triboelectric noise. Use thin wires for soldering to fanout pads on board.

Since most of the voltage measurements are associated with the copper traces, there is a question of whether deformation of the copper trace at the board surface can cause resistance changes. Quasi-static bending tests that do not cause solder joint cracks were performed to verify that the copper trace deformation does not cause significant measurement errors.

B.3 Effect of copper trace routing on measured resistance

Because a crack-induced voltage potential difference occurs over a continuum in the vicinity of the crack, a sensitivity study was performed to investigate the effect of crack location or orientation relative to where the current enters the pad (i.e. copper trace location), on electrical resistance across the joint. Figure B.1 shows the effect on resistance if the crack is positioned at various locations around the perimeter of the pad. Crack location induces a minor effect, due to the fact that both the crack and copper traces are constrictions to electrical current flow.

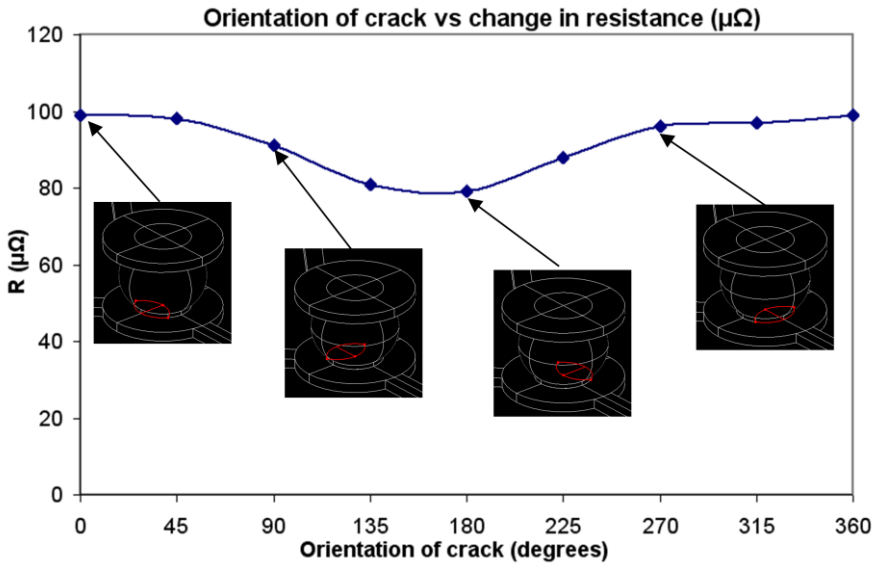


Figure B.1: Effect of crack location on electrical resistance across solder joint.

B.4 Effect of multiple cracks at component pad and board pad)

When a solder joint fails due to a complete crack along a pad, there is often a secondary partial crack along the pad at the other end of the solder joint, as shown in Fig B.2. A modeling study was performed to investigate the effect of a secondary crack on resistance measurements. Figure B.4 shows the effect of a combination of primary and secondary cracks on the resistance change across the solder joint. The primary crack is denoted by 'BL' indicating the 'bottom-left' position of the crack in Fig. B.2. The secondary crack is denoted by 'TR' indicating the 'top-right' position of the crack in Fig. B.2. The resistance increase due to the secondary crack is only significant when the size of the secondary crack is comparable to the size of the primary crack.

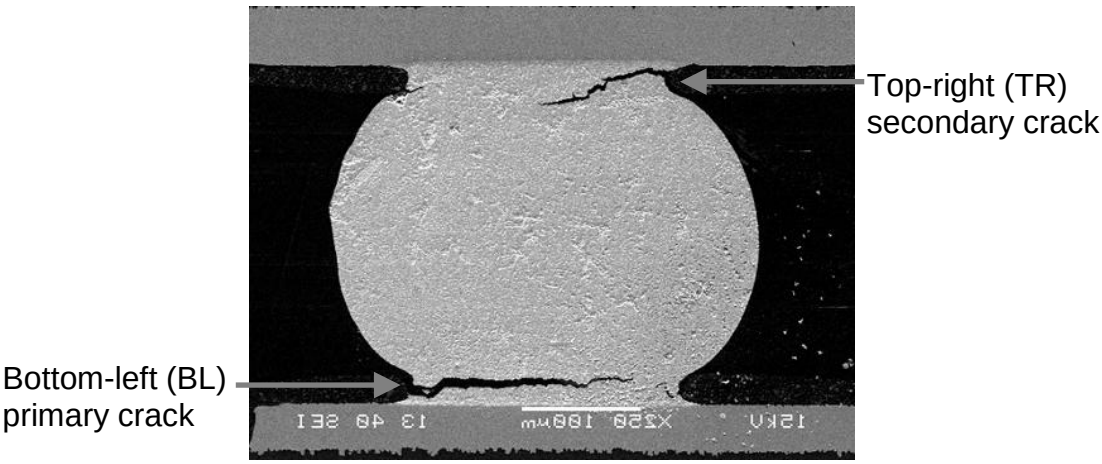


Figure B.2: Multiple cracks at both pads of a solder joint.

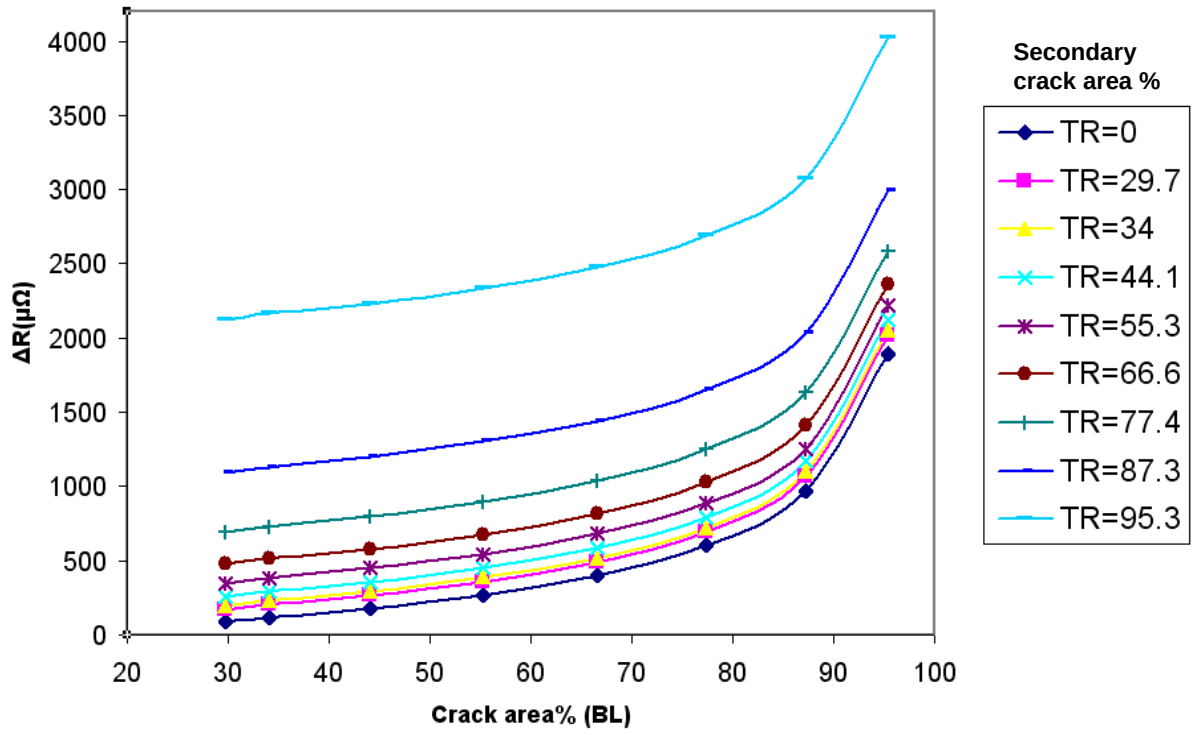
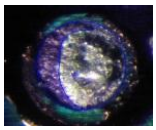
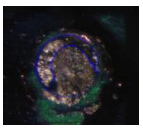
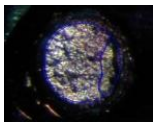
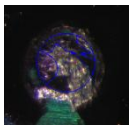
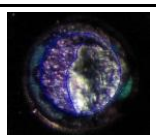
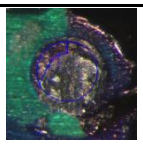
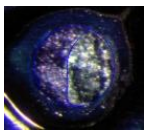
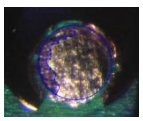
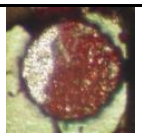
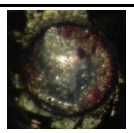
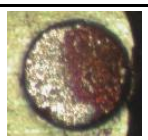
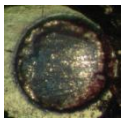
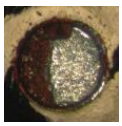
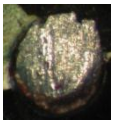


Figure B.3: Effect of primary crack (BL) and secondary crack (TR) sizes on electrical resistance across a solder joint.

B.5 Validation exercise

Table B.1 shows a comparison between the resistance change measured in experiments and the resistance change predicted from the model, for given crack areas observed in the experiments.

Table B.1: Comparison of measured resistance change from experiments and resistance change predicted from model.

Sample	**Board crack**	**Component crack**	**Measured Resistance change ($\mu\Omega$)**	**Predicted resistance change ($\mu\Omega$)**	**% diff**
Board 1			220	142	-35.4
Board 2			925	910	-1.5
Board 3			250	325	29.6
Board 4			220	235	7.0
Board 5			500	530	6.0
Board 6			170	210	23.9
Board 7			200	160	-20.0

B.6 Dye-and-Pry Tests

Dye-and-pry tests involve a “dyeing” step in which a liquid dye (Dykem Steel Red Layout Fluid) is applied to the component with cracked solder joints. Capillary action results in the dye entering the solder joint cracks. The sample is left to dry overnight or baked (at 100°C for 15 minutes), before a “prying” step is performed to separate the component from the PCB. The stained areas on the separated fracture surfaces indicate the extent of crack propagation.

To aid in the staining of the crack surfaces, the samples may be pre-bent slightly before application of the dye, to allow more dye to make contact with and stain the crack surfaces, as shown in Fig. B.4. Bending should be as little as possible to avoid inducing further crack propagation in the solder joints; in setup testing, strain gauges were used to ensure that the pre-bending strains are much lower (several hundred microstrains) than the test strains imposed to generate the cracks. Figure B.4 shows miniature paper clips used to pre-bend samples over a thin piece of spacer material. Other experimental steps explored included the use of forced air drying with a pneumatic air gun versus drying by natural convection. Forced air drying of the dye should be avoided because it tends to push the liquid dye out of the cracks. Fig. B.5 shows examples obtained from different dyeing and drying methods.

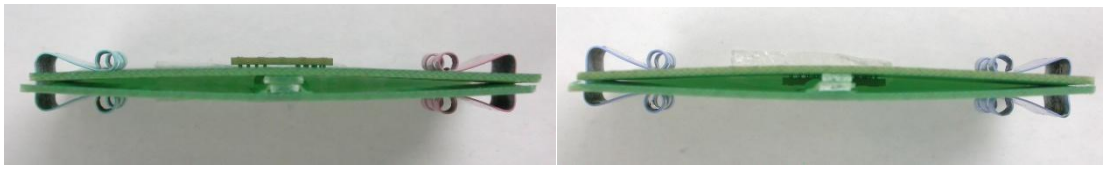


Figure B.4: Pre-bending of samples before dyeing step.

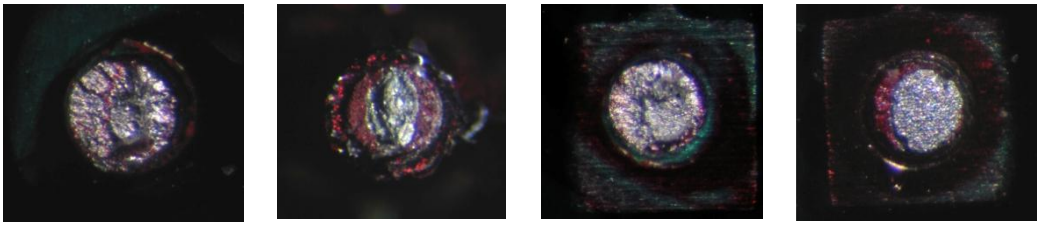


Figure B.5: Examples of dyed surfaces.

Several methods were also explored for separating or “prying” the component off the PCB. The most effective was found to be an impact bending method, illustrated in Fig. B.6, whereby a hammer is used to impart a blow to the PCB behind the component. This is to ensure a clean separation of the component from the PCB by inducing IMC failures at the solder joint. A slow prying of the component will result in extensive plastic deformation which may make assessment of the crack area difficult.

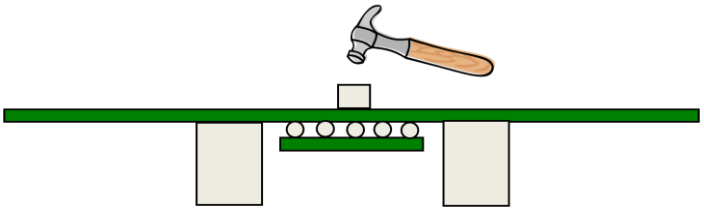


Figure B.6: Impact bending to separate component from PCB.

Appendix C

Test Method Development

C.1 High Speed Cyclic Bend Tester

A simple method for producing dynamic PCB bending is a drop/shock test on a fixture-mounted PCB that excites the natural frequencies of the PCB; this is the standard test method used in industry (Fig. C.1(a)). A typical PCB strain waveform generated in a drop test is shown in Fig. C.1(b). The waveform or loading history consists of a series of oscillations of decaying amplitudes. Each drop subjects the test vehicle to a unique loading cycle profile.

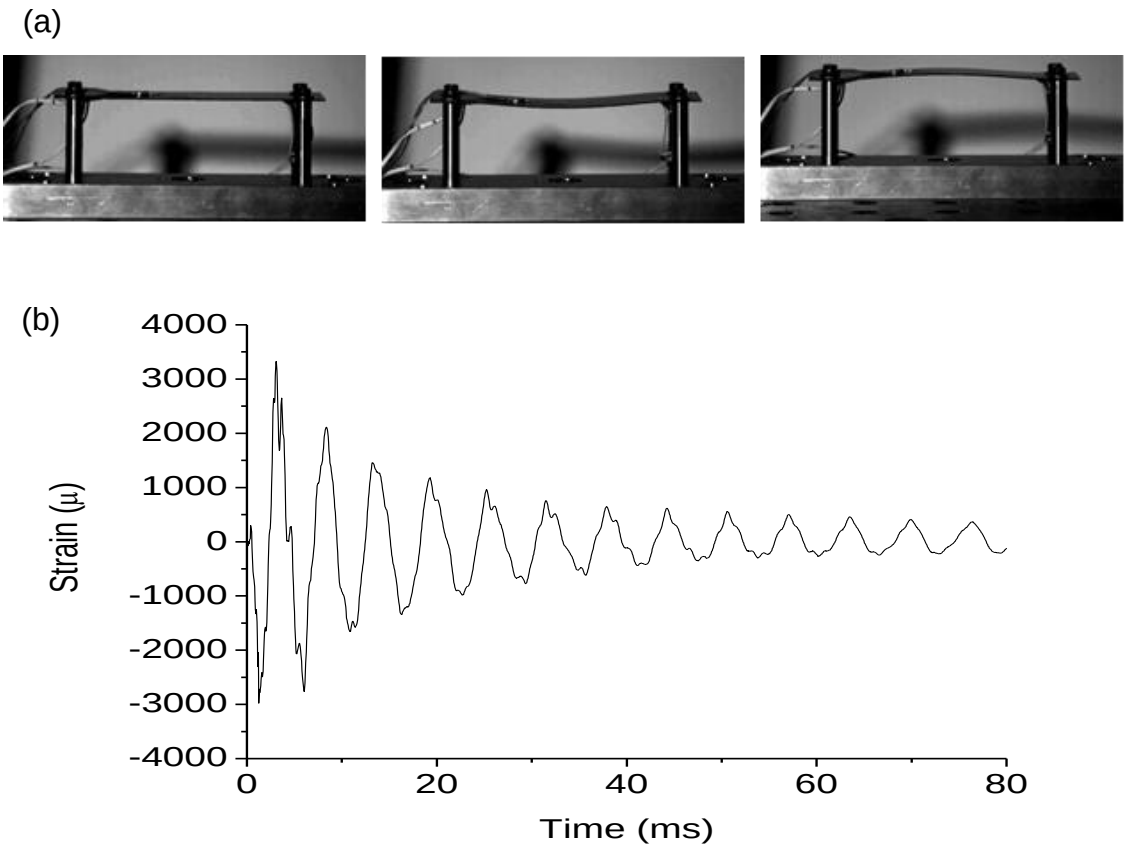


Figure C.1: (a) High speed camera images of a typical drop test with a fixture-mounted test vehicle (JEDEC drop test); (b) Strain waveform measured at center of test-vehicle during impact.

Based on the system level (portable electronic device) behaviour described in Chapters 1 and 3, it is clear that the loading history in a standard board level drop is completely different from the complex and highly variable loading histories in a system level drop test. The results from an industry board level drop test therefore have little relevance to how a mobile electronic product actually performs in the field. The results are at best useful for a relative comparison of performance between different solder material systems or components. In addition, because the standard JEDEC drop test method prescribes only a shock pulse to be applied in the test, the actual loads experienced by the joints vary significantly with fastening conditions and mechanical properties of individual boards.

The most versatile test method is one which can reproduce in a controllable manner, the individual elements of a complex load, namely the amplitude, frequency and numbers of bending cycles. Most universal mechanical test equipment (e.g. Instron, MTS) are unable to provide both the high displacement amplitudes and high cyclic frequencies required for reproducing strain levels similar to that observed in a drop impact event. A specially-designed high speed cyclic bend tester (HSCBT), prototype shown in Fig. C.2, was developed in collaboration with Instron (Singapore) Pte Ltd to provide this capability.

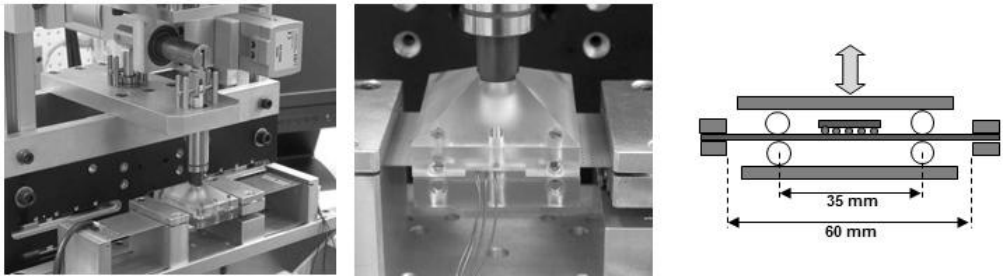


Figure C.2: High speed cyclic bend tester.

The tester developed applies displacements ranging from 0.5 to 5 mm to a bend test loading anvil. The loading anvil is connected to a lever which in turn is connected to a motorized rotary cam that generates sinusoidal motion. Instead of standard sinusoidal motion, other load histories, or blocks of loading cycles, may be profiled onto the cam. Test frequencies can be varied between 10 and 300 Hz, and single cycle loading is possible with the use of a brake and clutch system to limit the cam to producing a single bending load cycle. The high speed bend tester therefore allows a controlled characterization of fatigue performance of solder joints under variable amplitudes and frequencies. PCB strain pulses generated by the tester are shown in Fig. C.3.

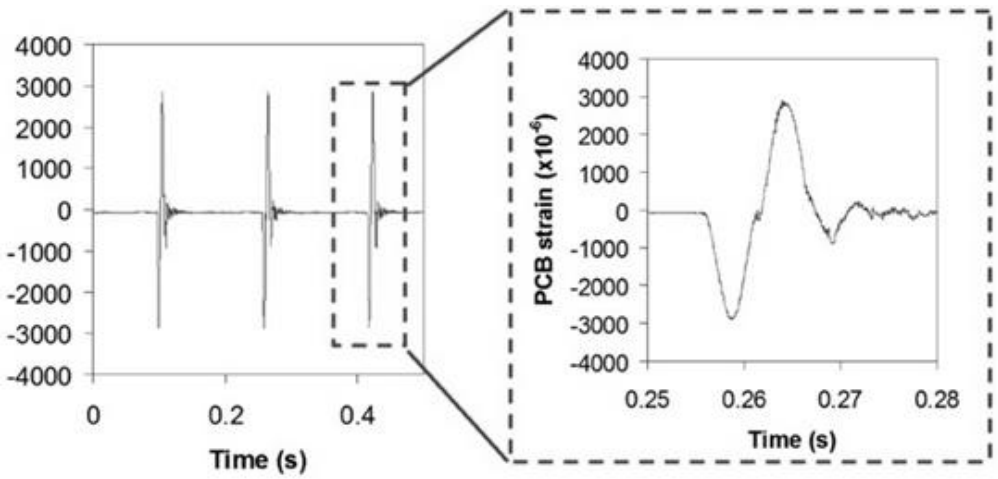


Figure C.3: PCB strains during cyclic bend testing.

C.2 Comparison of half-sine with sinusoidal load cycles

While full sinusoidal cycles are the loads typically applied in laboratory fatigue tests, in reality, PCB strains experienced by mobile devices in drop impact are typically half-sine in shape. Figure C.4 shows examples of PCB strains measured during the drop impact of mobile phones. Other examples of half-sine loads can be seen in Fig. 3.4 of Chapter 3.

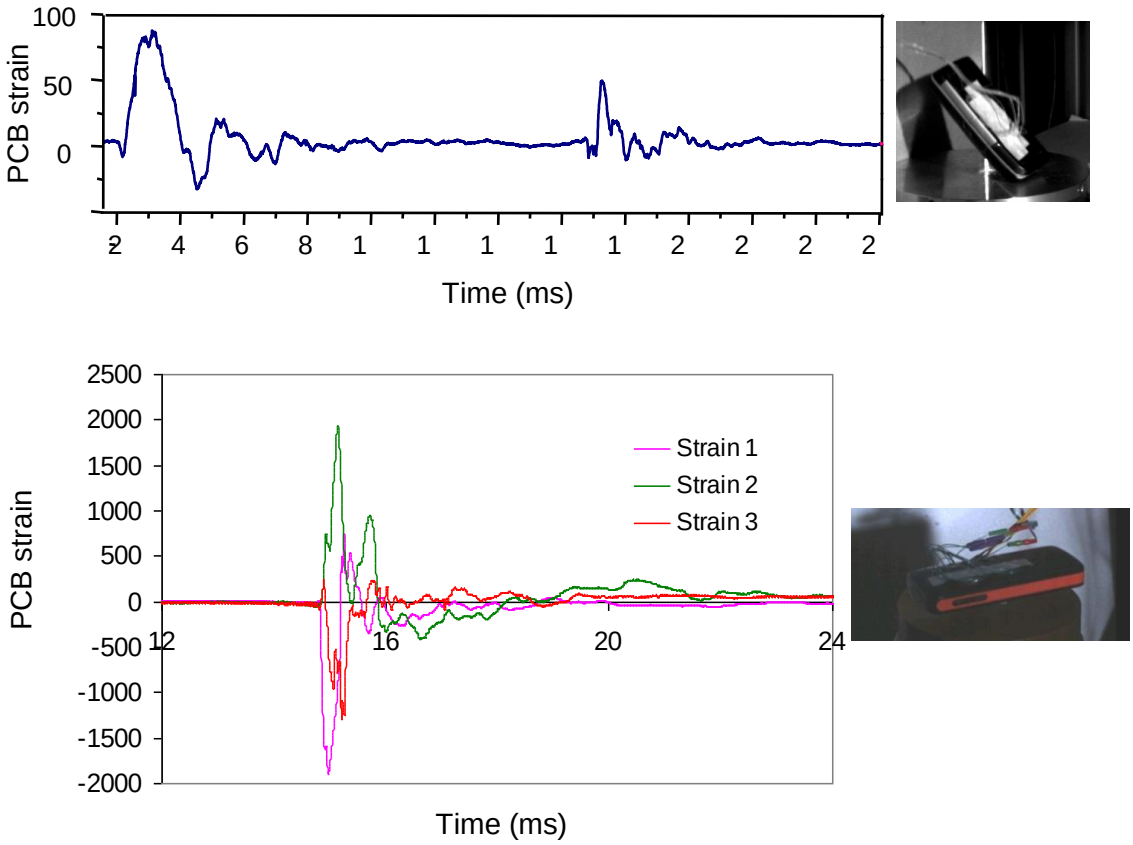


Figure C.4: PCB strains measured during drop impact of mobile phones.

A study is performed to compare the fatigue life of solder joints under half-sine and full sinusoidal PCB strains. To produce full sinusoidal strains, the HSCBT is used. To produce half-sine strains, the plunger impact setup shown in Fig. C.5 is used. While it is possible for the HSCBT to generate half-sine cycles if assembled

with a half-sine cam, the plunger impact setup is used in this study to limit costs. This test is more difficult to control than the HSCBT, but is usable for handling a limited range of parameters. The mass of the plunger and support span are adjusted to achieve a bending frequency of 100 Hz. Figure C.5 shows half-sine pulses generated in a plunger impact test. The solder joint used is SN100C-Cu.

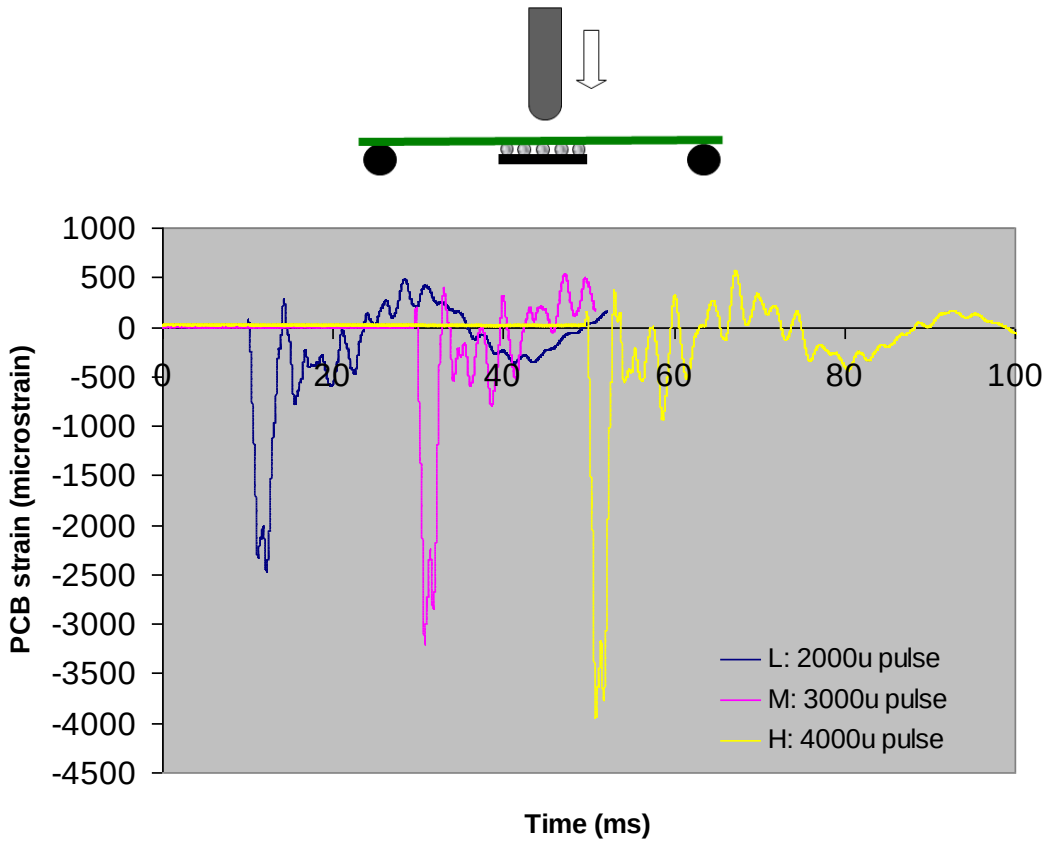


Figure C.5: Half-sine bending pulses from plunger impact tests.

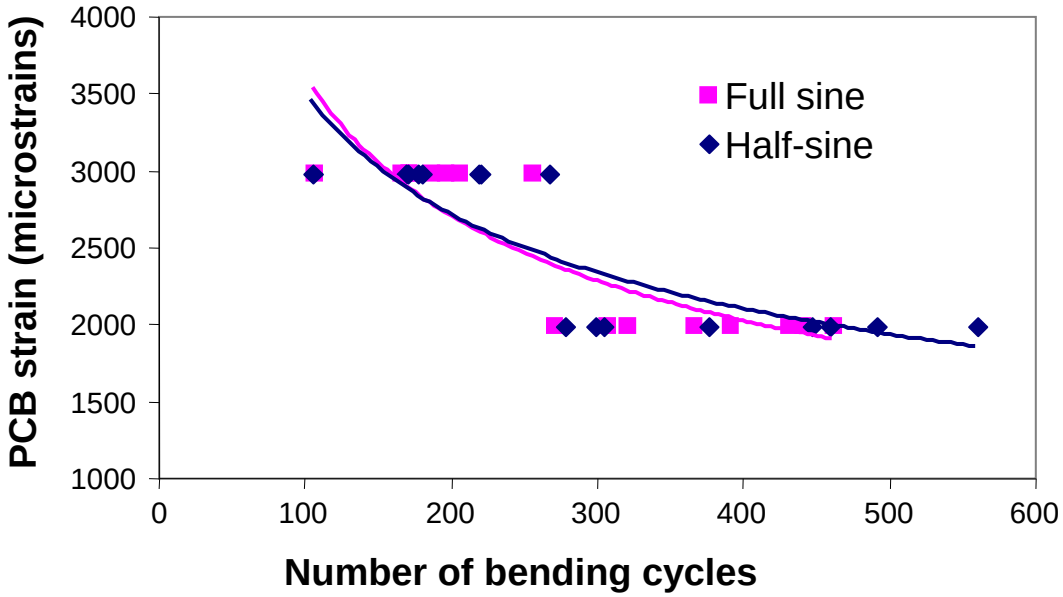
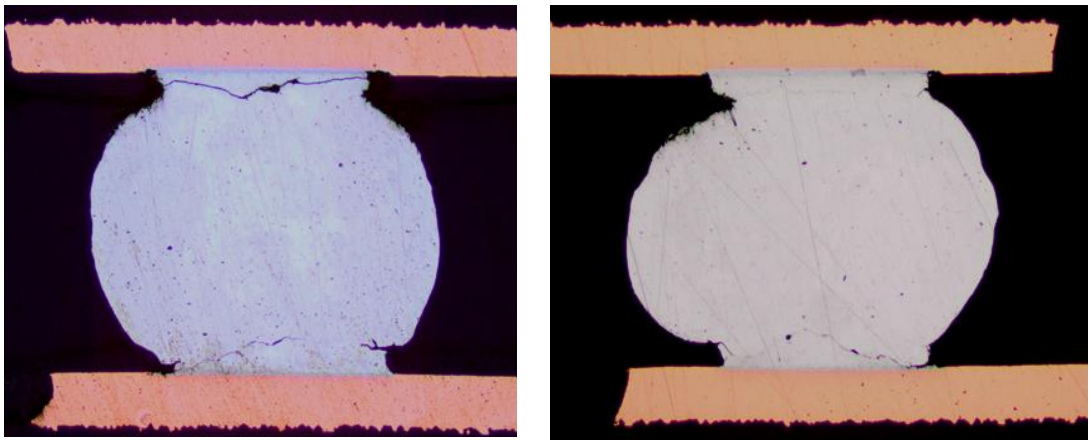


Figure C.6: S-N curves obtained from HSCBT and plunger impact tests (100 Hz).

Figure C.6 shows a comparison between the S-N curves obtained using half-sine and sinusoidal loads. Very similar fatigue life characteristics are seen, suggesting that only the tensile part of the load cycle causes damage in the solder joints. The failure modes are also similar, as shown in Fig. C.7, which compares cross-sections from the two tests. Half-sine bending pulses also produce cracks at both the PCB and component sides of the solder joint. The cracks for the samples loaded by a half-sine pulse appear to be hairline-thin, likely due to the absence of compressive contact of the crack surfaces.

Half-sine



Full sine

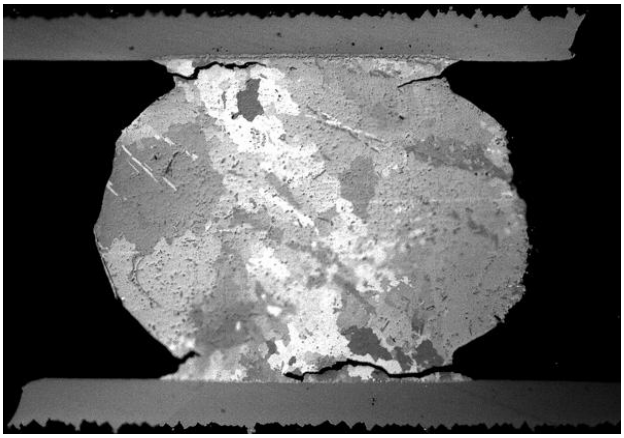


Figure C.7: Failure modes from (a) half-sine tests; (b) full-sine tests.

Appendix D

Error Analysis of Fatigue Data

Tables D.1 and D.2 present the mean values and relative error (standard deviation) for each test condition or dataset in the test matrix. The numbers in parentheses indicate the sample size for each test condition. Table D.1 shows that SN100C on Cu/OSP is the most robust and consistent solder joint material system. Error analysis of Table D.2 indicates that the data spread generally increases with higher bending frequencies and amplitudes. This pattern is linked to an increase in IMC failures at higher bending frequencies and amplitudes. It is hypothesized that IMC failure leads to a more random distribution in cycles-to-failure, because there is much more variation in the patterns associated with the formation of IMC layers, compared to the bulk solder material in a joint.

Table D.1: Mean and relative error for Study of Materials Influence (100 Hz). Sample size for each dataset is indicated in parentheses.

Solder \ **Pad**	**Cu / OSP, 2000µ**	**ENIG, 1200µ**
SN100C-0.6%Cu	355 ± 13% (12)	597 ± 60% (16)
SN100C-0.8%Cu	366 ± 17% (16)	546 ± 66% (16)
SAC305	57 ± 79% (8)	356 ± 53% (12)
SnPb	226 ± 11% (8)	511 ± 56% (12)
SAC101(Ni doped)	336 ± 30% (12)	617 ± 75% (16)

Table D.2: Mean and relative error for Study of Strain/Frequency Influence.
Sample size for each dataset is indicated in parentheses.

Material system: SAC101 on Cu/OSP				
Frequency / PCB Strain (μ)	**30 Hz**	**50 Hz**	**100 Hz**	**150 Hz**
1000	-	-	927 ± 42% (20)	-
1200	1306 ± 39% (12)	926 ± 49% (20)	783 ± 49% (32)	191 ± 37% (12)
1500	745 ± 28% (12)	499 ± 55% (20)	279 ± 71% (24)	142 ± 94% (28)
1800	408 ± 38% (12)	329 ± 54% (20)	211 ± 84% (24)	80 ± 98% (24)
2100	279 ± 50% (12)	275 ± 63% (24)	245 ± 40% (20)	32 ± 190% (12)
2400	135 ± 96% (12)	191 ± 80% (20)	266 ± 41% (20)	29 ± 121% (12)
2700	-	-	70 ± 120% (20)	-
Material system: SN100C on Cu/OSP				
Frequency / PCB Strain (μ)	**50 Hz**	**100 Hz**	**200 Hz**	**300 Hz**
2000	450 ± 16% (8)	366 ± 17% (16)	230 ± 34% (8)	121 ± 14% (4)
3000	248 ± 21% (8)	181 ± 23% (8)	86 ± 37% (8)	27 ± 59% (4)

Of particular note are the results in Table D.2 for SAC101-Cu/OSP (100 Hz) for strains of 1500μ and 1800μ, which cannot statistically be shown to be from different test conditions. These test conditions may require a larger sample size to obtain statistically meaningful results. In general, data scatter increases when there are mixed mode failures in the dataset. For comparison, data scatter from a study on low-cycle fatigue life of dogbone solder samples [26] is shown in Fig. D.1.

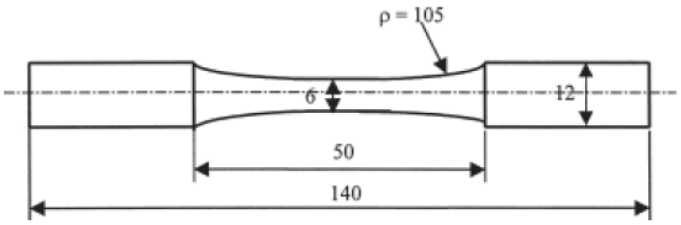


Fig. 1. Geometry of fatigue specimen (unit: mm).

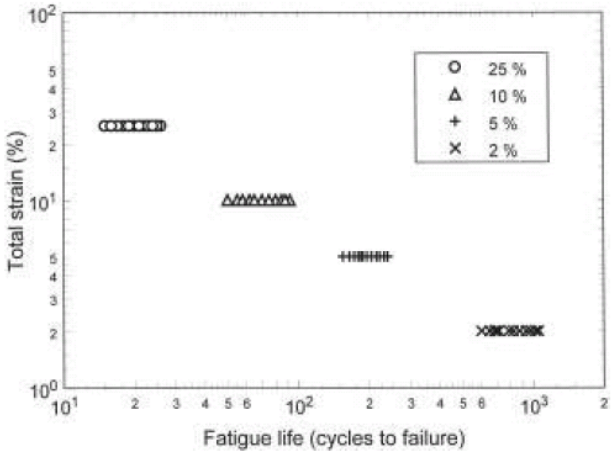


Fig. 2. Total strain range versus fatigue life at 25°C and 1 Hz.

Figure D.1: Example of data scatter from a previous solder fatigue life study on creep-dominated fatigue (Shi et al.) [26].

The SN100C-Cu/OSP material system shows very consistent results, even for a relatively small sample size. Therefore, the SN100C-Cu/OSP material system is used for the life prediction modeling, in order to maximize use of the limited PCB sample material available.

Screening of solder joint shape and size using cross-sectioning was also performed for each batch of samples fabricated, to check that there were no serious deviations in the manufacturing process. Figure D.2 shows several cross-sections of solder joints which, despite their variability, are all well-formed high-quality joints. Nonetheless, the ultimate test of manufacturing process reliability is mechanical performance consistency. While some production environments may perform 100% checks of the dimensions of *unsoldered* bumps of components, this is impractical or impossible for soldered joints of PCB assemblies. Instead, manufacturers perform destructive shear tests or bend tests on sample batches of board assemblies to assess the consistency of the board assembly process. The excellent consistency of the HSCBT fatigue test results for SN100C-Cu/OSP samples indicates a well-controlled manufacturing process. Variations in test results are much more likely to be a consequence of randomness in IMC formation, rather than minor variations in solder joint shapes and sizes.

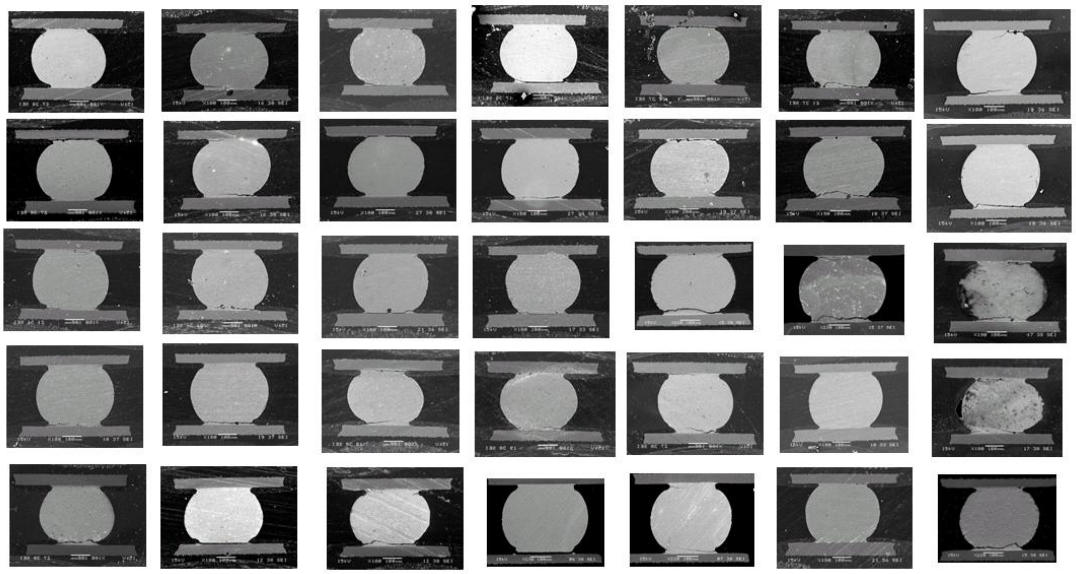


Figure D.2: Cross-sections of typical solder joints used in fatigue tests.

Appendix E

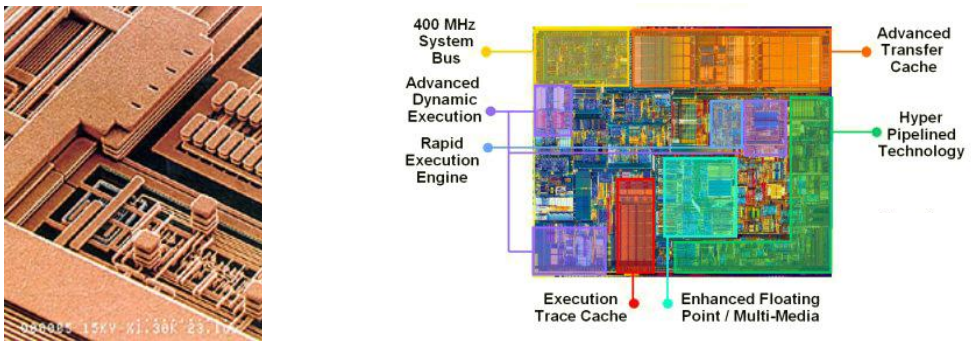
(From M.Eng thesis [2], updated to include recent technologies)

An Introduction to Electronic Packaging Technology

The field of microelectronics began in the 1960s with the invention of a technique of fabricating tiny circuit elements, namely transistors, on thin slices or ***wafers*** of a semiconducting material. Each wafer piece containing a miniature ***integrated circuit*** (IC) is called a ***die*** or more commonly, a chip, and is housed in an ***electronic package***. Being an integral part of the chip-making process, electronic packaging has been in constant evolution throughout the short history of microelectronics. Advances in both wafer fabrication technology and package design have been driven by the demand for smaller, cheaper, faster and more energy-efficient electronic products.

Introduction to the manufacture and use of chip packages

In a typical chip-making process, a wafer of semiconducting material – usually silicon – is subjected to oxidation to form a thin layer of insulating silicon dioxide on its surface. The basic structures of the transistors and circuit patterns are formed by selectively removing parts of this insulating layer. ***Photolithography*** and ***etching*** – the prevailing methods used today to form minute features – are used to form these structures. ***Doping*** is performed to impart certain electrical characteristics to the exposed silicon. These processes may be repeated numerous times to build up, in several layers, the entire electronic circuitry in the wafer. ***Thin films***, which form conducting lines (Fig. 1(a)) among different regions (Fig. 1(b)) of the wafer, are deposited towards the end of the wafer fabrication process. Finally, a protective ***passivation layer*** is deposited on the wafer. Openings are etched in the passivation layer to form conductive ***pads*** for external connections to and from the die. The dimensions of the structures formed in the wafer fabrication process are in the order of submicrons. For example, the "0.09 micron" and "0.13 micron" processes often advertised by chip manufacturers today are directly related to the width of the transistor gates and the thickness of the conducting lines.



(a) (b)

Figure 1: (a) Layers of thin film lines on a silicon wafer [1]; (b) Architecture of an Intel Celeron die showing different functional regions [2]

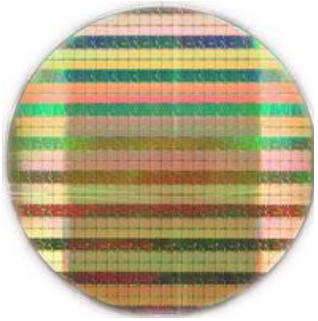


Figure 2: Entire silicon wafer consisting of numerous chips

The finished wafer (Fig. 2) is then tested for functionality before being diced or ***singulated*** into individual chips. This ends the ***front-end process*** of chip fabrication. The ***back-end process*** involves housing each chip within a package. A wide variety of package designs are available, but all serve five important functions: 1) for protection of the chip from the environment; 2) for providing electrical connections between the chip and the outside world; 3) for physical attachment of the chip to supporting structures; 4) for conducting heat away from the dense electrical circuitry in the chip; and 5) for ***redistributing*** the high-density circuitry within the chip to lower-density circuitry outside the package. Packaged chips undergo further testing before being shipped to their immediate users, which are the manufacturers of computers, portable telecommunication equipment and other electronic products.

During the manufacture of an electronic product, chip packages are soldered to ***printed circuit boards (PCBs)***, also known as ***printed wiring boards (PWBs)*** (Fig. 3). The process of attaching packages to the board is called ***board assembly***. Embedded in several layers within a PCB (Fig. 4) are networks of copper ***lines*** or ***traces*** that electrically connect the packages and other components on the PCB.

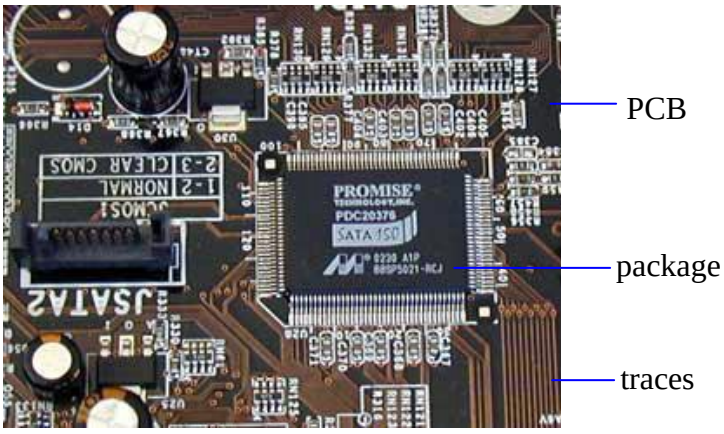


Figure 3: Top surface of PCB assembly [3]

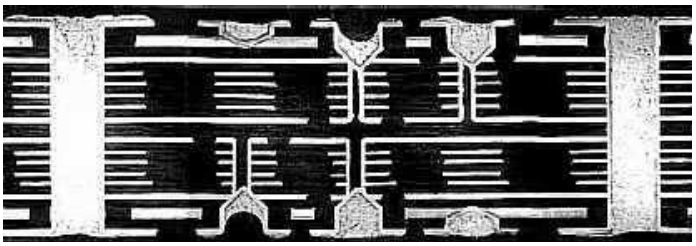


Figure 4: Cross-section along edge of PCB showing the conductive trace layers [4]

Electronic products may consist of a single PCB, in the case of many of today's mobile phones, or several PCBs connected together, in the case of computers. Since a break anywhere along the chain of electrical connections from die to PCB will result in a loss of product functionality, much research has been dedicated to ensuring the reliability of every aspect of die, package and PCB. This project is concerned specifically with the reliability of the ***solder joints*** or ***interconnections*** between the package and the PCB. In electronic packaging jargon, the package-to-PCB bonding is also known as ***Level 2 Packaging*** (Level 0 and Level 1 denote the die and die-to-package levels respectively, while Level 3 and above denote PCB-to-PCB and product-to-product packaging).

Evolution of electronic package design

Early electronic package designs were based predominantly on ***through-hole technology (THT)***. Through-hole board assembly involves attaching packages to PCBs by placing their ***leads*** into ***plated through holes (PTHs)*** (Fig. 5) in the PCBs. This is followed by a process called ***wave soldering*** (Fig. 6) in which a liquid wave of molten solder is passed along the bottom of the board to achieve bonding between leads and holes. An example of a through-hole package is the familiar ***dual in-line package (DIP)***, shown in Fig. 7.

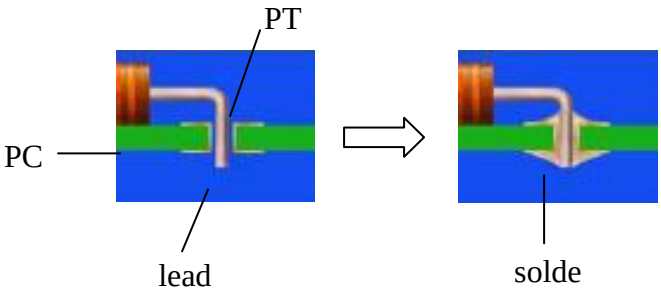


Figure 5: Through-hole technology: lead soldered in PTH [5]

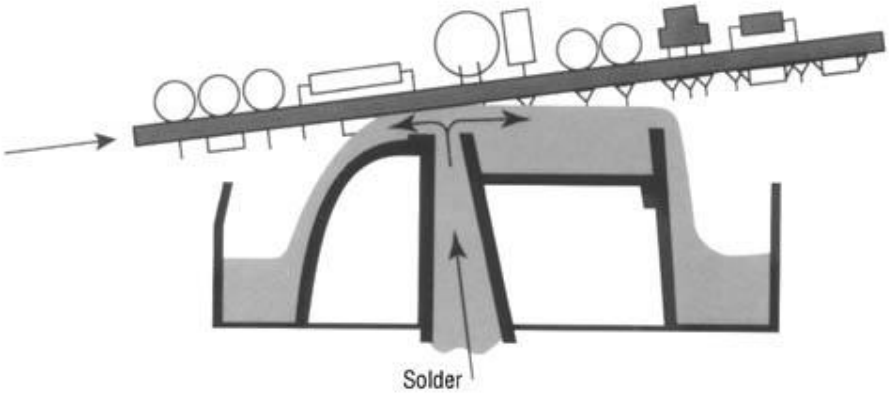


Figure 6: Schematic of wave soldering [6]

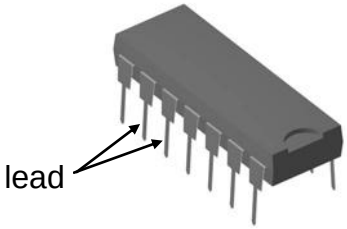
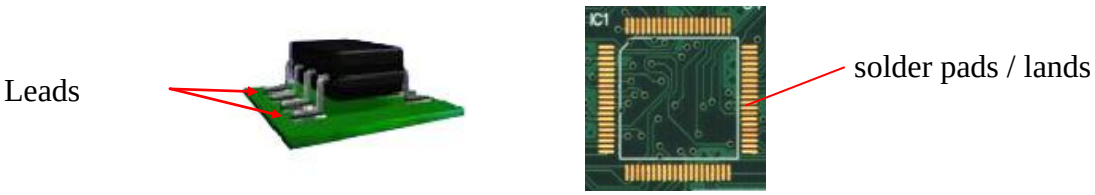


Figure 7: Dual in-line package (DIP)

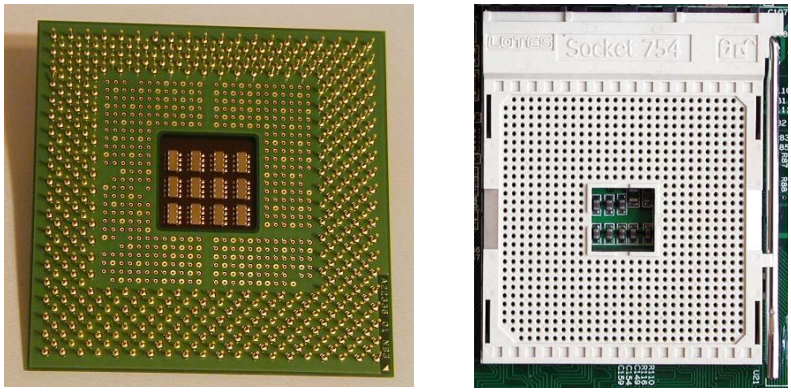
However, THT is inefficient in the use of board space or “real estate" because holes need to be made through every copper layer in the PCB, and traces have to be routed at least a minimum distance from holes. In the drive towards denser circuitry, the limits of THT were soon reached. Manufacturers responded to these limitations by adopting ***surface mount technology (SMT)***. ***Surface mount assembly (SMA)*** is performed by soldering package leads to pads or ***lands*** on the surface of the PCB (Fig. 8).



(a) (b)

Figure 8: (a) SMT package mounted on PCB [5]; (b) Pads for surface mounting of package [4]

Surface mount packages are also lighter and, due to their shorter leads, have better electrical performance. Although SMT has almost completely replaced THT, through-hole packages are still used, especially in applications requiring large electrical currents and/or strong mechanical bonding between package and PCB. Through-hole packages are also used when easy installation and removal of packages is required, as in the case of the socket-installed, ***pin grid array (PGA)*** central processor packages of today's desktop computers (Fig. 9).



(a) (b)

Figure 9: (a) Pins of Pentium 4 processor package [7]; (b) Socket of AMD 754-pin processor [8]

With SMT arrived a new family of chip packages, complete with a new set of acronyms by which they are called. Several early surface mount packages, such as the Small Outline Integrated Circuit (SOIC) (Fig. 10) and the Small Outline J-leaded package (SOJ), are essentially DIPs, except that their leads are bent into shapes suitable for surface mounting. Leads may be bent into ***gull wing leads*** or ***J-bend leads***, shown in Fig. 11. For a higher ***lead count*** or ***input/output (I/O) count***, leads could be arranged along all four edges of the package, as in the Plastic Leaded Chip-Carrier (PLCC) and the ***Quad Flat Package (QFP)*** (Fig. 12).

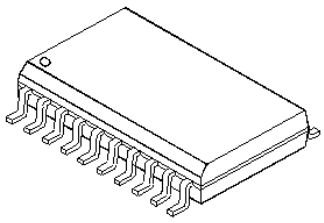
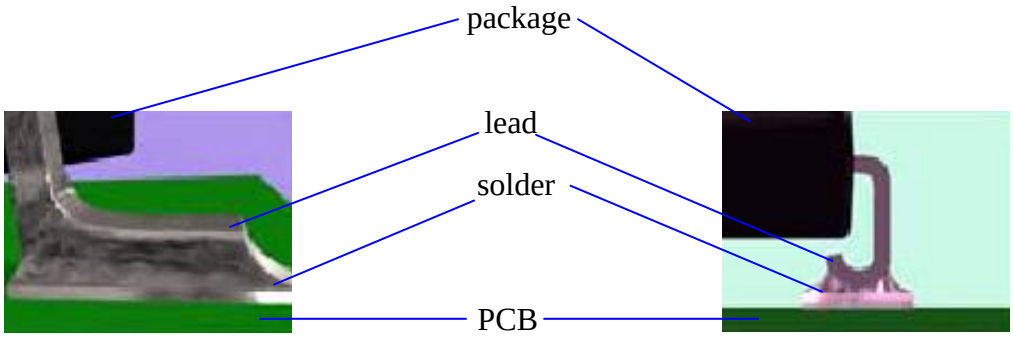


Figure 10: SOIC with gull wing leads [9]



(a) (b)

Figure 11: (a) Gull wing lead [10]; (b) J-bend lead [10]

(a) (b)

Figure 12: (a) PLCC (with J-bend leads) [11]; (b) QFP (with gull wing leads) [12]

The packages in Figs. 10 and 12 are examples of ***lead frame*** packages. Lead frame packages are constructed by bonding a die to a metal frame composed of a mounting ***paddle*** and ***lead fingers***, as shown in Fig. 13. Mechanical bonding between die and lead frame is achieved using a carefully selected ***die attach*** material, the key properties of which are moisture resistance, adhesion strength, elastic modulus, thermal conductivity and processing temperature. Die attachment is followed by a ***wire bonding*** process in which gold or aluminium wire is strung from conducting pads on the chip to the lead fingers (Fig. 14). A less popular alternative to wire bonding is ***tape automated bonding (TAB)***. After wire bonding or TAB, the die is either enclosed in a plastic ***encapsulant*** or sealed within a ceramic package body. Finally, the exposed leads are bent into the desired shapes (either gull-wing or J-bend), thus completing the package (Fig. 15).

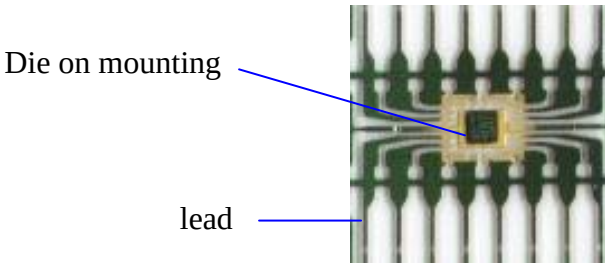


Figure 13: Construction of lead frame package [13]

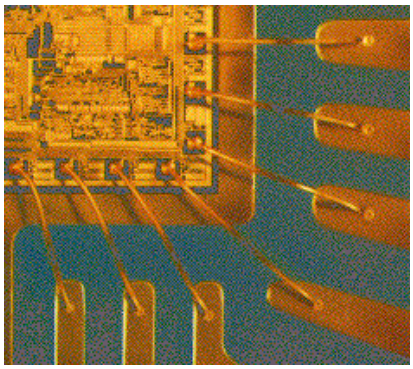


Figure 14: Wire bonding of chip to lead fingers

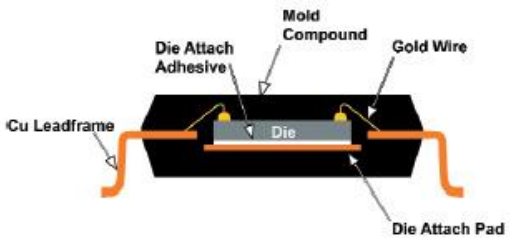


Figure 15: Side view schematic of SOIC [14]

In the manufacture of ***plastic packages***, the die is typically encapsulated in transfer-molded plastic epoxy. In general, encapsulant materials are chosen based on properties such as coefficient of thermal expansion (CTE), flexural strength, flexural modulus, glass transition temperature, moisture resistance, ultimate strain and susceptibility to ***warpage***. While plastic epoxy is the most common encapsulant, ***ceramic packages*** are used extensively for military and aerospace applications where high performance, high reliability and hermeticity are required, since ceramics have a low permeability to water, and are resistant to corrosion and high temperatures.

Further improvements in circuit density could be achieved by increasing the sheer number of leads without substantially increasing the physical dimensions of the package. Therefore, the distance between adjacent leads, called the lead ***pitch***, began to shrink. The term ***fine pitch*** was coined to describe packages with a pitch of less than 0.635 mm or 25 ***mil***. Pitch may be specified in either millimeters or mils (one mil equals one thousandth of an inch), but if convention is to be strictly followed, only a pitch smaller than 20 mils is specified in millimeters, while a pitch larger than 20 mils is specified in mils. Examples of fine pitch packages are the thin small outline package (TSOP) and the fine pitch quad flat package (FPQFP) which, respectively, are the fine pitch counterparts of the SOIC and QFP. The design, manufacture and use of fine pitch packages require sufficiently more sophisticated techniques than previously required for "conventional" SMT packages. These advanced techniques are collectively termed ***fine pitch technology***.

Ultimately, even fine pitch QFPs are not the best solution for increasing the number of I/Os per given board area. Major shortcomings of such packages are that the leads are restricted to the periphery of the package, and soldering is much more difficult with fine, delicate and closely-spaced leads. Further progress was made possible with the introduction of the ***ball grid array (BGA)*** package (Fig. 16). Instead of having peripheral leads, a BGA package has solder balls distributed or ***populated*** over the area of its bottom surface.

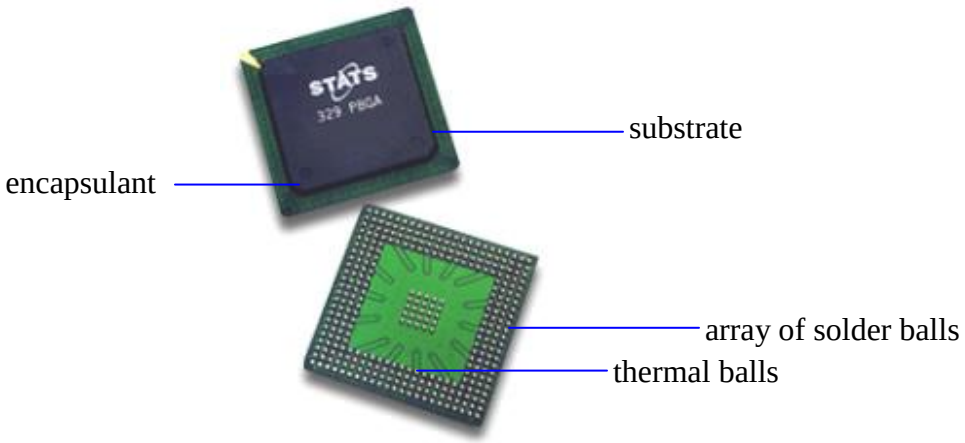
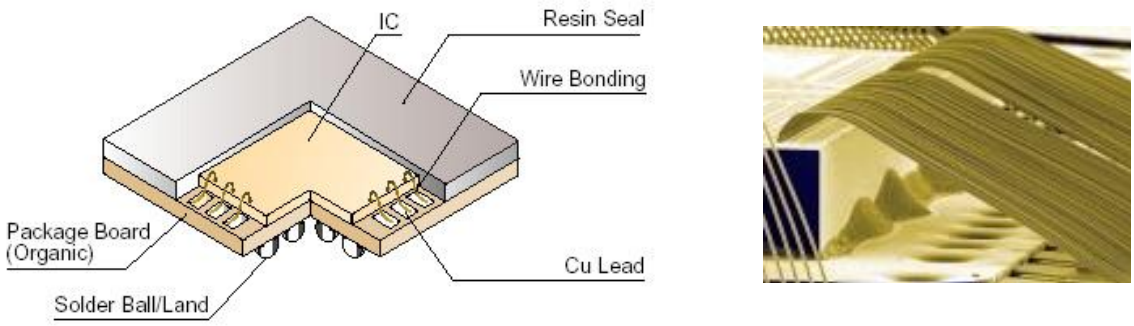


Figure 16: BGA package [15]

In the production of a BGA package, the die is first mounted on a base, called a ***substrate*** or ***chip carrier***, using a carefully selected die attach material. Wire bonding is typically performed to electrically connect the die to wire bond pads on the substrate (Fig. 17). Conductive lines within the substrate begin at the wire bond pads, and end at the solder ball array on the surface of the substrate. After wire bonding, a molding process is performed to encapsulate the die and the top surface of the substrate.

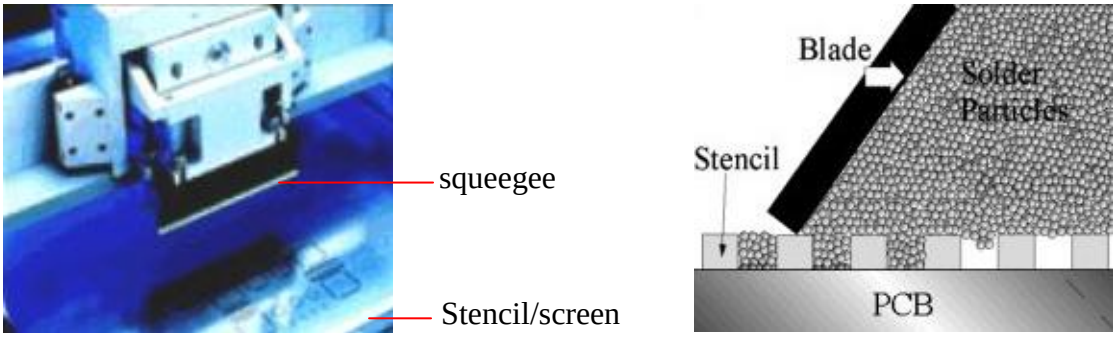


(a) (b)

Figure 17: (a) Schematic of BGA package showing wire bonding [16]; (b) Wire bonds from chip to substrate [17]

BGA packages have several advantages over QFPs. The use of a substrate instead of the flimsy lead fingers of lead frame packages is found to result in fewer manufacturing defects during wire bonding and subsequent molding. Manufacturing defects are reduced during board assembly as well, because solder balls are larger and more robust, and the pitch of a BGA package is typically larger than that of an FPQFP with the same I/O count. The coarser pitch allows greater tolerances during the placement of the package on the PCB. Board space is also saved because for a given I/O count, BGA packages are normally smaller than QFP packages. However, the higher I/O density means that the routing of the traces in the PCB is more complicated. There are also improvements in electrical performance, owing to the shorter electrical connections within the substrate, and the short length of the solder balls. BGA packages typically have better thermal performance because heat may be conducted away through ***thermal vias*** that connect the die directly to ***thermal balls*** (Fig. 16) at the bottom of the substrate. The only major disadvantage of BGA packages is that inspection and repair of solder joints is difficult or impossible, since the joints are hidden underneath the package.

BGA and other SMT packages are normally attached to PCBs using a series of processes, namely, ***solder paste*** printing, ***component placement*** and ***reflow soldering***. Solder in the form of a paste – composed of solder particles, flux and solvent – is first ***stencil printed*** or ***screen printed*** (Fig. 18) onto the conductive pads of a PCB. These processes involve using a squeegee to push the paste (Fig. 19(a)) through the openings in a ***stencil*** (Fig. 19(b)) or ***screen*** placed over the board.



(a) (b)

Figure 18: (a) Stencil/screen printing [18]; (b) Schematic of stencil printing [18]

(a) (b)

Figure 19: (a) Solder paste being pushed by squeegee [18]; (b) Stencil with openings for QFP solder pads [18]

Component placement is then performed with a ***pick-and-place*** machine that typically uses a vacuum-suction nozzle to pick up the components/packages, and a camera-based optical alignment system to position the components accurately on the pads. With the sticky solder paste holding the packages in place, the PCB is placed on a conveyor belt that enters a ***reflow oven*** (Fig. 20). As it slowly passes through the oven, the board is subjected to a set of varying temperatures, also called a ***reflow profile*** / ***solder profile*** / ***thermal profile***. The reflow profile is carefully engineered to prevent thermal damage to components and to produce solder joints having reliable metallurgical characteristics. When the solder balls and solder paste underneath the BGA package reach their melting point (183 °C for eutectic Pb-Sn solder), they collapse to form the shapes of the solder joints. Surface tension determines the shape of a solder joint. Surface tension also supports the weight of the package, keeping a certain height between the package and the PCB, and helping to align the BGA pads with the PCB pads should there be any inaccuracies in the pick-and-place process.

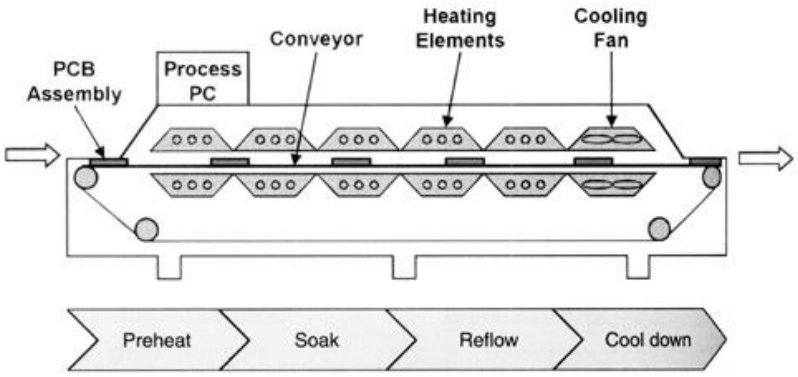


Figure 20: Schematic of reflow soldering [19]

One of the limitations of BGA package design is that wire bond pads of the chip are located only on the periphery, and the chip occupies only a small region at the center of the substrate, as shown in Fig. 21. In this case, the chip is much smaller than the overall package. Improvements in the wire bonding process allowed bond pads to be spaced closer together and nearer the die, and tighter wire loops to be made between die and substrate (Fig. 22). Eventually, the substrate could be shrunk to a size only slightly larger than the chip, thus giving rise to the term ***chip scale package (CSP)***. A CSP is defined as a package having a size that is at most 1.2 times the size of the die. It should be noted that the term CSP simply denotes the size of the die relative to the package and not the package type. CSPs may come in the form of lead frame or area array packages, although they are usually the latter.

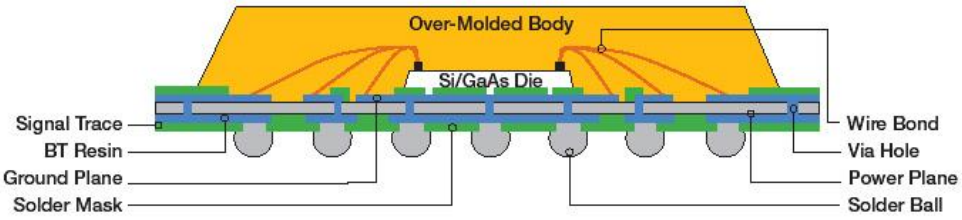


Figure 21: Side view schematic of wire bond BGA package [20]

Figure 22: Tight wire loops of a CSP [21]

Ultimately, wire bonding is still limited to the periphery of the chip. This situation is analogous to leaded packages having only peripheral leads. ***Flip-chip (FC) attachment*** provides a means for overcoming this limitation. In flip-chip attachment, solder bumps on the area of a chip face are used to connect chip to substrate (Fig. 23), much like BGA solder balls are used to connect package to PCB. During attachment of chip to substrate, the populated face is flipped over onto pads on the substrate, hence the term "flip-chip". Flip-chip involves bonding the die in a ***face down*** configuration, as opposed to a ***face up*** configuration in wire bonding.

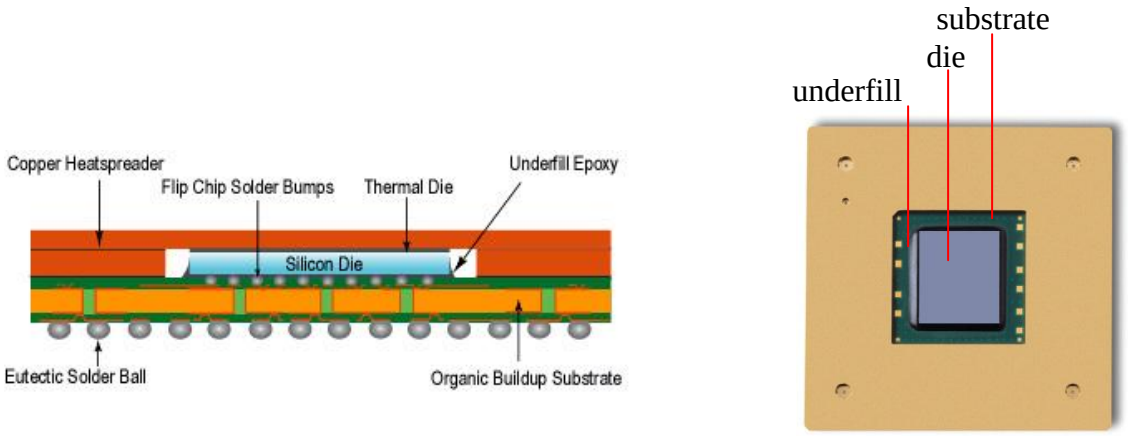


Figure 23: (a) Side view schematic of flip-chip BGA package [22]; (b) Top view of a flip-chip BGA package [23]

Flip-chip technology was introduced as early as the 1960s when it could be more economical than the manual wire bonding that was used at that time. It has taken on a greater importance today as a possible successor to wire bonding in the push towards higher connection densities. Although the solder bumps on a flip-chip die may seem akin to solder balls at the bottom of a BGA substrate, there are significant differences in how they are manufactured and used. In flip-chip manufacture, careful considerations are given to the interface between the solder bumps and the conducting pads on the die. Before formation of the solder bumps, a sequence of several different thin films, called the ***under bump metallisation (UBM)***, is layered onto the die pads. Each layer in the UBM serves a certain purpose, such as improving adhesion and solderability, reducing corrosion and oxidation, and preventing problems such as brittle intermetallic formation that is caused by excessive intermetallic diffusion through the interface between solder and pad. There are several options for attaching a flip-chip die to the chip substrate. Flip-chip dies may be connected to substrates in a similar way as BGAs are attached to PCBs, that is, by placement of the die onto the substrate pads followed by reflow. **C*ontrolled collapse chip connection (C4)*** is a common term used to describe the complete melting of Level 1 eutectic solder bumps during the reflow process. An alternative to C4 is using a high-melting-point solder for the bumps, but a lower-melting-point solder as the bridge between bump and substrate pad. Adhesives containing conductive particles may also be used for flip-chip attachment. ***Isotropic conductive adhesives*** applied between the solder bumps and pads serve the dual purpose of providing mechanical adhesion and electrical conductivity. ***Anisotropic conductive adhesives*** differ from the isotropic type in that electrical conductivity is obtained only if the adhesive is subjected to a certain

compressive force. Anisotropic conductive adhesives are applied to the whole area under the chip and not only on the pads. The adhesive regions that are squeezed between the bumps and pads conduct electric current while the regions between the bumps do not, hence the term "anisotropic". Conductive adhesives are still the subject of much research as they suffer from several reliability problems. However, they are advantageous in that they 1) require low processing temperatures; 2) are able to bond to almost any material; and 3) in the case of anisotropic adhesives, have the triple role of adhesive, electrical conductor and ***underfill*** encapsulant. An underfill encapsulant is an epoxy that is used whenever flip-chip solder connections are made between a high CTE ceramic die and a low CTE substrate. Underfills serve as additional bonding between the die and substrate (Fig. 23) and absorb some of the stresses in the solder bumps during ***thermal cycling***, thereby improving fatigue life. After flip-chip attachment and underfill encapsulation, the die may be fully encapsulated as usual. Flip-chip technology provides the advantages that accrue to an area array technology. A notable disadvantage is that extra concern has to be placed on thermal fatigue of Level 1 solder joints, because bumps of small heights are more vulnerable to stresses caused by thermal cycling.

The latest development in packaging technology is ***wafer-level packaging (WLP)***. WLP takes a radically different approach of packaging the chips on the wafer, even before singulation. The back-end process is therefore integrated into the wafer fabrication process. WLP can result in huge cost reductions because packaging and testing are done only at the wafer level. Thin film conducting lines within the die redistribute the dense circuitry in the chip to coarse Level 2 interconnections that can match the pad density of the PCB. Because Level 2 interconnections are formed directly on the die without the use of a substrate, a wafer level CSP (Fig. 24) is practically the same size as the die; it would therefore be smaller than lead frame, wire bond or FC CSPs having the same I/O count. Wafer-level packages are also different in certain mechanical aspects. For example, the large mismatch between the CTEs of a (mostly) ceramic wafer-level package and an organic PCB necessitates the development of various compliant Level 2 interconnections.

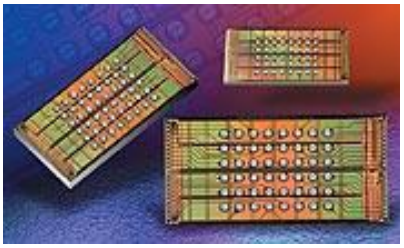


Figure 24: Wafer level package [24]

PCBs and substrates

The construction of a typical organic PCB begins with a fiber-reinforced composite prepreg. During curing of the prepreg, a sheet of copper foil is pressed against one or both sides of the prepreg to form a conductive layer (Fig. 25) in which the circuit patterns will be etched. A ***positive mask*** is then applied to the copper surface to cover and protect the areas that will later make up the pads and trace patterns. After positive mask formation, chemical etching is performed to remove the copper that is not covered by the mask, thus forming the conductive patterns. If the circuit patterns are coarse, screen printing is sufficient for transferring the mask. However, high-density patterns such as ***fine line circuitry*** – where the trace width is less than 7 mils – requires the higher-resolution process of photolithography. The photolithographic process is fundamentally the same as that used in chip fabrication. The process involves the 1) deposition of a photosensitive material, called ***photoresist***, onto the copper, followed by 2) exposure of selected parts of the photoresist to light passing through a photographic film, called a ***photomask***, which contains an image of the circuit pattern (Fig. 26). UV light passing through the photomask chemically changes the photoresist, making it either susceptible or resistant (depending on the preferred process) to a chemical ***developer***. The developer dissolves the weak portions of the photoresist in order to form the mask pattern.

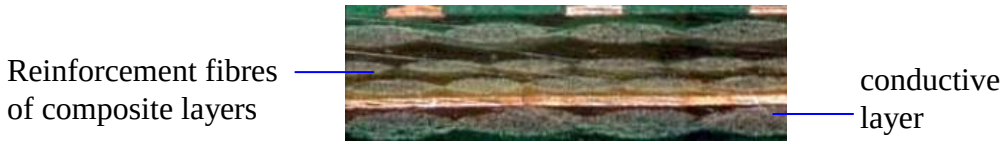
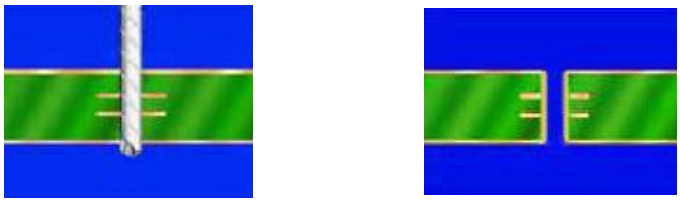


Figure 25: Conductive layer within a PCB

Figure 26: Exposure of photoresist [10]

Although the widely-used ***subtractive process*** of etching away the unwanted copper gives the best copper-to-prepreg adhesion, an ***additive process*** using a ***negative mask*** can be used for directly electroplating the copper trace patterns. The additive process is commonly used because it avoids wastage of copper. Whether they are additive or subtractive, the above steps may be repeated to form a ***multilayer PCB*** consisting of several composite prepreg layers alternating with conductive copper layers. Electrical connections between different layers of copper are achieved using conductive holes. The construction of these holes begins with mechanical drilling at selected locations on the PCB (Fig. 27(a)). Copper metal is then chemically deposited along the surface of the holes in an ***electroless plating*** process. Subsequent ***electroplating*** further builds up the copper metal (fig. 27(b)). The resulting conductive holes are called ***vias*** or PTHs, ***blind vias*** and ***buried vias*** (Fig. 28).



(a) (b)

Figure 27: (a) Drilling of hole [10]; (b) After plating of hole [10]

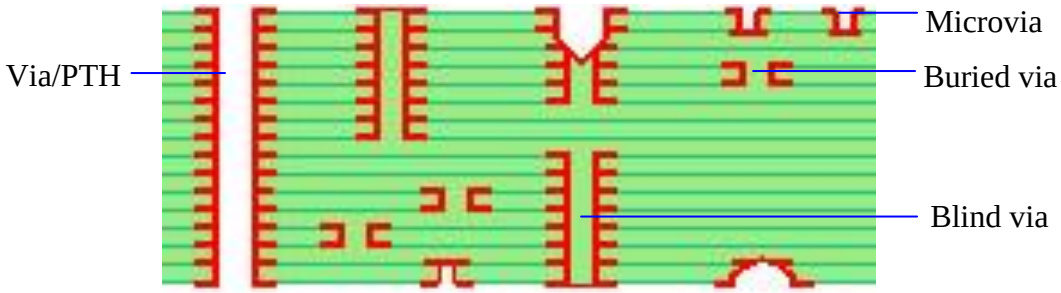


Figure 28: PTHs, blind vias and buried vias [4]

Electroplating is also performed to deposit other metals, such as tin-lead, nickel and gold onto copper pads. These metallizations will 1) improve the solderability of copper pads; 2) protect the copper against the environment; and 3) prevent unwanted diffusion of metals and other chemical species through the pad surface during soldering. The final step in PCB manufacture is the application of a layer of ***solder mask*** or ***solder resist*** onto the surface of the PCB. Solder mask has the primary function of preventing solder deposition on all areas of the board except the pads, and secondary functions of insulating, protecting and improving the appearance of the outer board layers. Solder mask is particularly important in situations where the pitch is very fine, as it prevents the "bridging" of solder across adjacent pads. Solder mask may also be used to define the exposed areas of the conductive pads on the PCB, as shown in Fig. 29. ***SMD*** (solder-mask-defined) pads have solder mask openings that are smaller than the pads. ***NSMD*** (non-solder-mask-defined) pads have solder mask openings that are larger than the pads. SMD pads are believed to have better adhesion to the PCB due to the solder mask overlapping the outer edges of the pads. However, the stress concentrations in solder joints at the overlap regions are found to reduce the cycles-to-failure in thermal fatigue conditions. Therefore, NSMD pads are generally preferred today because they increase the fatigue life of solder joints.

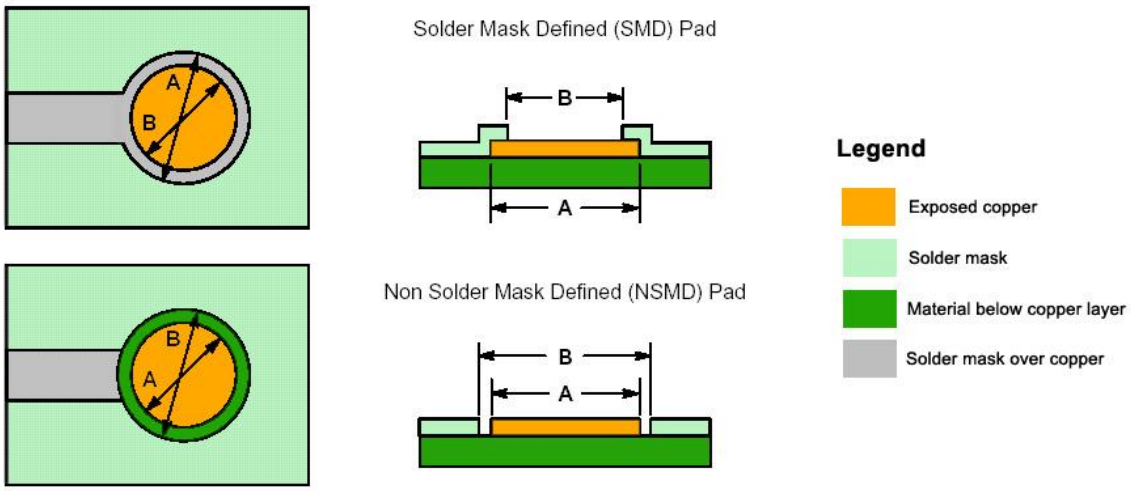


Figure 29: SMD and NSMD pads [25]

The processes described above for the manufacture of PCBs may also be used to manufacture organic BGA substrates, because both PCB and package substrates have the same function of containing conducting lines. However, substrates typically have higher density requirements and may be made of other materials besides organic composites. A wide variety of PCB and BGA substrate materials exist, ranging from flexible polymer films and fiber-reinforced composite laminates to ceramic materials. Various factors affect the selection of a substrate for use in a certain application. The most common material used for PCBs is ***FR-4***, a "flame retardant" grade of composite laminate consisting of fiberglass cloth in an epoxy matrix. Although FR-4 is cheap, moisture-resistant, and allows good copper adhesion, its electrical properties are not good enough for high-speed applications, such as for BGA substrates. Instead, the most common material used for BGA substrates is the more costly bismaleimide-triazine, or ***BT resin***. BT resin is preferred because it has better electrical characteristics and thermal performance. The higher glass transition temperature T_g of BT ensures that material properties and physical dimensions remain stable at high temperatures. The lower coefficient of thermal expansion (CTE) of BT resin is closer to that of the silicon die, which means lower stresses in the region between the die and substrate when the package experiences thermal cycles of heating and cooling. Other key properties of BT resin, such as moisture resistance and copper adhesion, are comparable to those of FR-4, moisture resistance being important to ensure that absorbed moisture does not create delamination when the package is heated (the ***popcorn effect***), and copper adhesion being important to ensure sufficient pull strength of the copper pads. If robustness and hermeticity are necessary, ***multilayer ceramic*** substrates are used. If a thinner or ***low profile*** package is required, a thin flexible polyimide film, called a ***flex substrate***, can be used as the substrate. Flexible substrate packages are used often in the production of mobile phones and other small products where slim and small are major requirements. It should be noted at this point that the term "substrate" is used rather liberally at all levels of electronic packaging. During wafer fabrication, the silicon base is the substrate; during die packaging, the base for mounting the die is the substrate; during board assembly, the PCB is sometimes termed the substrate. The meaning of the term is therefore derived from the context.

Substrate designs employing mechanically drilled vias are sufficient only to a certain extent. This is because there are manufacturing limitations on how small and close together holes may be drilled. As pitch, via diameter and pad size decrease, it becomes exponentially more costly and difficult to drill and also plate the tiny holes required for via formation. Among the latest advances in electronic packaging are ***microvia*** technologies. Microvias can be described as blind or buried vias, typically smaller than 6 mils in diameter, which are manufactured not by mechanical drilling, but higher-resolution processes such as ***laser ablation***, photolithography or ***plasma etching***. The pads on the top of a microvia are usually much smaller than 25 mils or 0.635 mm in diameter. The small sizes allow increased pad and hole density without sacrificing "between-pad" space for routing the traces and without increasing the number of conductive layers in the substrate. Microvia boards are often synonymous with ***High-Density Interconnect (HDI)*** boards or ***build-up boards*** or ***Surface Laminar Circuit (SLC)*** boards. As their name implies, build-up boards are composed of layers of microvias that are built up on a conventional PCB base. (Fig. 30).

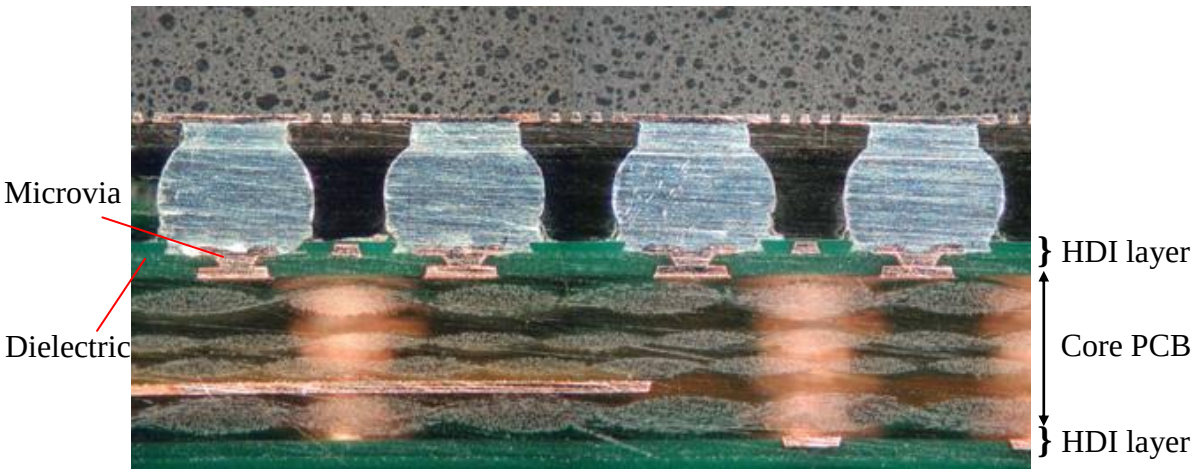


Figure 30: HDI layer on PCB core

The first step in the manufacture of microvias is the deposition of a thin dielectric layer onto the surface of a ***core PCB*** (Fig. 30) that is typically a normal FR-4 PCB. It is within this dielectric layer that the microvias are formed. Copper trace patterns are then formed on top of the dielectric layer using either an additive or subtractive process. The tiny holes required for microvia formation may be produced using laser ablation where a laser beam is used to punch out tiny holes through the copper and dielectric layers. A cheaper but less flexible method is photolithography where the dielectric material behaves as a photoresist and has holes etched into it. Yet another method for making holes is plasma etching where small plasma fields composed of highly reactive ions are generated in a low-pressure environment to chemically attack the board surface. Whichever method is used, holes are finally plated using electroless copper deposition and, if necessary, subsequent electroplating. Microvias created using laser ablation, photolithography and plasma etching are called ***laservias***, ***photovias*** and ***plasmavias*** respectively. The above processes may be repeated to form multiple HDI layers, as shown in Fig. 31. A build-up board is often described by a series of numbers that indicates the number of conductive layers in the board. For example, a build-up board having a 2-4-2 configuration has 2 microvia layers on one

surface of the board, 4 conductive layers within the core PCB, and 2 microvia layers on the other surface of the board.

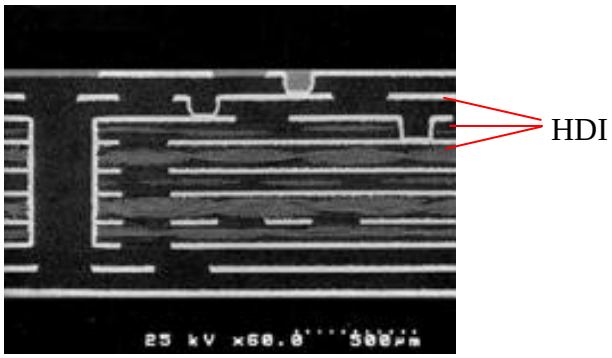


Figure 31: Multiple HDI layers [26].

Current and future advanced chip packaging solutions

The technologies described above are the basic components and manufacturing processes used in electronic packaging today. Many variations exist, and many more are actively being developed. For example, Level 1 packaging can be removed completely through the use of ***Direct Chip Attach (DCA)*** where the die is bonded directly to the PCB without any packaging or redistribution. Instead of housing a single chip, electronic packages called ***multi-chip modules (MCMs)*** can house several chips as well as ***passives*** (e.g. resistors and capacitors) (Fig. 32). MCMs are a precursor to ***SIP (system-in-package)*** where an entire electronic system can be housed in a package. SIP together with ***SOC (system-on-chip)*** and ***SOP (system-on-package)*** are advanced solutions for integrating as much functionality into as small a package as possible. Figure 33 shows the four basic approaches to integrate a full electronic system onto a single component [28]. ***Vertical integration*** or ***3-D packaging*** technologies allow silicon dies to be stacked vertically and interconnected. For example, 3-D packaging technologies are a key enabler of ever increasing capacities of USB flash memory thumb drives [29]. An example of stacked flash memory dies is shown in Fig. 34, which uses ***through-silicon vias (TSVs)*** to interconnect the dies, instead of wire-bonding which is exceedingly challenging for large stacks of dies. Many excellent reports which track the current and future trends in electronic packaging technologies are available [30]. Figure 34 shows a summary of package and substrate technologies that have been developed in recent years [30].

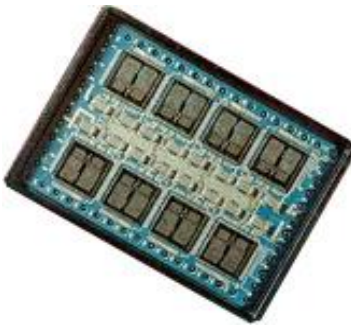


Figure 32: MCM [27]

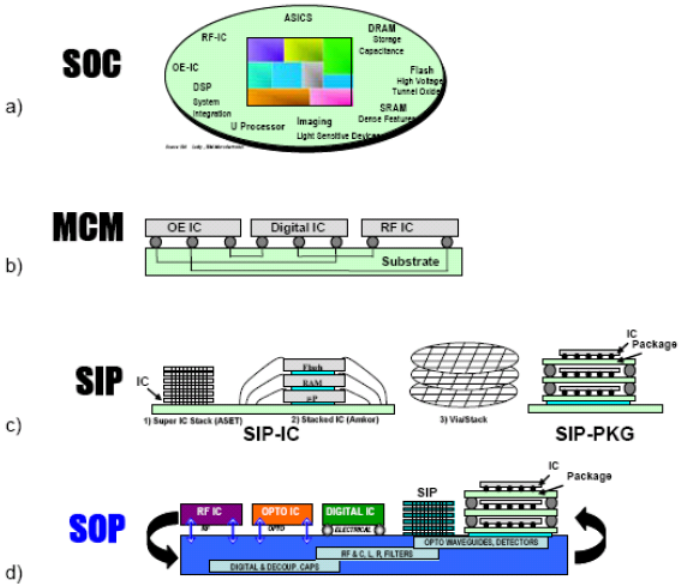


Figure 33: Four approaches to integrate a system on a single component [28].

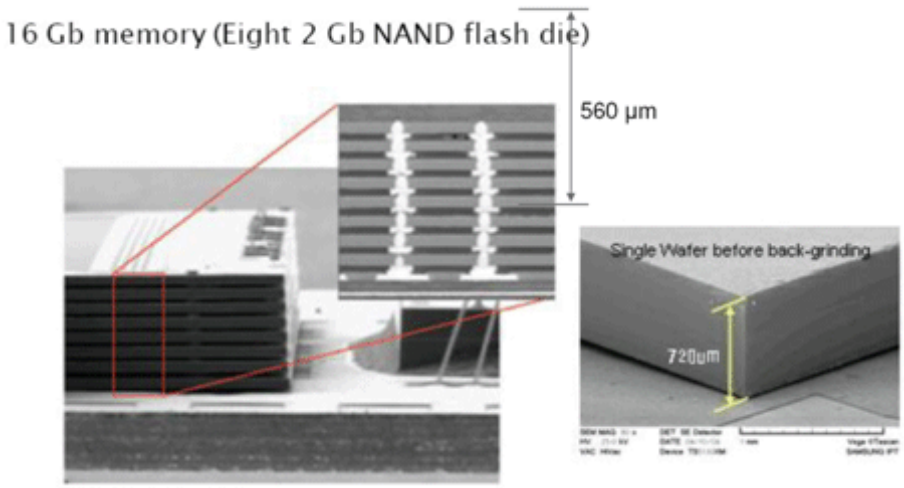


Figure 34: Stacked memory dies using through-silicon-vias (TSVs). Source: Samsung.

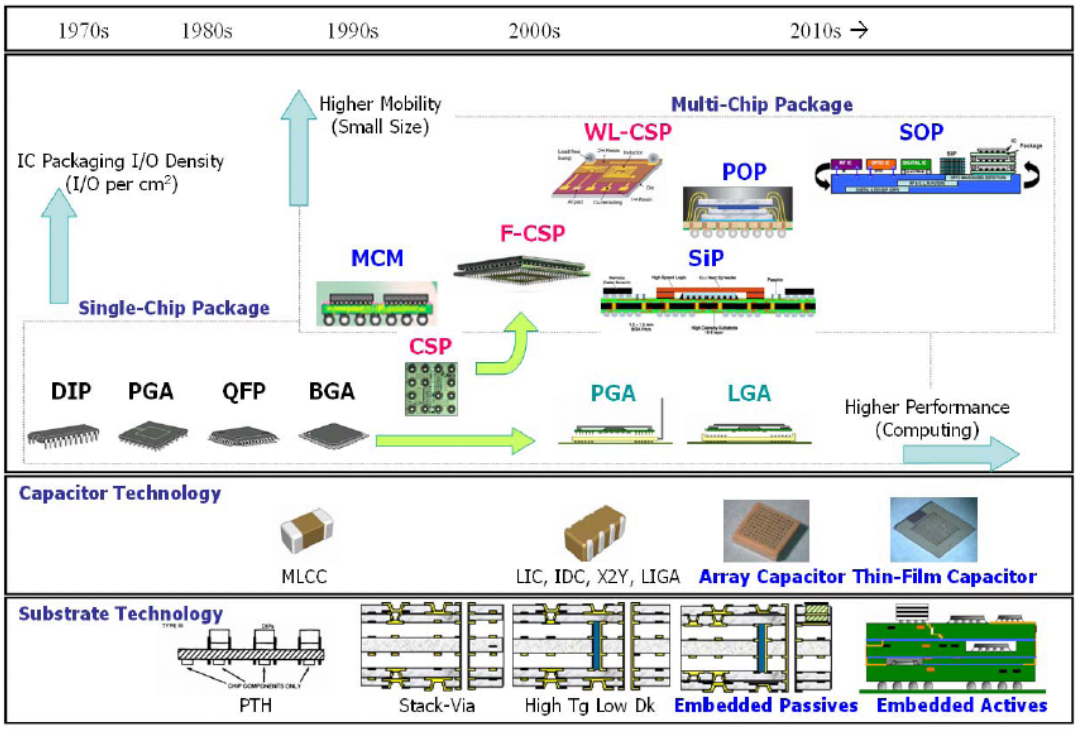


Figure 35: Current and future trends in electronic packaging [30].

Glossary of terms

additive process
The process of directly plating or depositing circuit patterns, as opposed to etching out the patterns.

anisotropic conductive adhesive
An adhesive material that contains conductive particles. Sufficient pressure has to be applied in a certain direction for the material to conduct electricity.

area array
Describes the distribution of interconnections over the area of a chip or substrate, as opposed to peripheral interconnections.

back-end process
A collective term for the processes by which chips are housed within packages.

BGA
Short for Ball Grid Array, BGA is a type of package that has area array solder balls as Level 2 interconnections.

blind via
A conductive hole that leads from the surface of the substrate to a layer within the substrate.

board assembly
The process in which components are attached to PCBs. Also used to describe a PCB that has undergone the board assembly process.

BT resin
Short for bismaleimide-triazine, BT resin is commonly used in package substrates because of its excellent electrical and mechanical properties.

build-up board
A substrate which is composed of microvia layers built up on a core PCB.

buried via
A conductive hole that is embedded within the substrate; it links only internal layers of the substrate.

C4
Short for Controlled Collapse Chip Connection, C4 describes the complete melting of Level 1 solder bumps during flip chip attachment.

ceramic package
A package that has a ceramic substrate. Glass- or metal-sealed with a ceramic lid for hermeticity.

chip
A piece of material containing an integrated circuit. Also known as a *die*.

chip carrier
The base onto which the die is attached. Also called by the more general term "package substrate".

CSP
Short for Chip Scale Package, CSP is a class of packages that have an overall size that is at most 1.2 times the size of the chip.

DCA
Short for Direct Chip Attach, a type of packaging or attachment that eliminates Level 1 interconnections.

die
See *chip*.

die attach
The adhesive material that is used to mechanically bond the chip to a substrate or lead frame.

DIP
Short for Dual In-line Package, DIP is a package type that has interconnection pins aligned along two parallel edges.

electroless plating
A metal deposition process that occurs by chemical reaction and does not require an electrical current.

encapsulant
The material used to encase the chip after Level 1 interconnections have been formed. Also known as *molding compound*. Sometimes used to refer to *underfill*.

etching
The process of "carving out" patterns and features in a layer of material.

FC
Short for Flip Chip, FC attachment involves forming solder bumps on the surface of the die and flipping this surface over onto the substrate for attachment of die bumps to substrate pads.

fine line circuitry
Circuit patterns that have a trace width of less than 7 mils.

fine pitch
Packages with a pitch of less than 25 mil.

flex substrate
A thin flexible polymer tape on which circuit patterns are laid.

FR-4
A "Flame Retardant" grade of material which is commonly used in PCBs.

front-end process
The wafer fabrication process.

gull wing lead
A lead which is bent into a shape which resembles a gull wing.

HDI
Short for High Density Interconnect. See *build-up board*.

I/O count
Short for input/output count, I/O count refers to the number of (Level 2) interconnections, be it leads or solder balls, of a package.

IC
Short for Integrated Circuit, an IC is a tiny electronic device that contains numerous circuit elements and can perform various electronic functions. ICs today are built on semiconducting material such as silicon.

interconnection
A general term describing any structure which forms an electrical and/or mechanical link.

isotropic conductive adhesive
An adhesive material which conducts electricity owing to the presence of embedded conductive particles.

J-bend lead
A lead which is bent into a shape which resembles the letter J.

land
See *pad*.

laser ablation
A method in which a laser beam is used to punch out tiny holes through copper and dielectric layers during microvia formation.

laservia
A microvia formed using laser ablation.

lead count
See *I/O Count*.

lead frame
A piece of sheet metal which is composed of 1) a base for mounting the chip; and 2) the structures of the leads.

leads
The slender interconnections between a lead frame package and a PCB.

Level 1 packaging
The interconnections between the chip and the substrate / lead frame.

Level 2 packaging
The interconnections between the package and the PCB.

line
See *trace*.

MCM
Short for "Multi-Chip Module", MCM is a class of packages which contain multiple chips as well as passives.

microvia
Small conductive holes that are manufactured not by mechanical drilling, but by higher-resolution processes such as laser ablation, photolithography or plasma etching.

mil
One thousandth of an inch.

molding compound
See *encapsulant*.

multilayer PCB
A PCB that has alternating prepreg and conductive layers.

negative mask
A mask which exposes the desired circuit patterns. May refer to a photomask or the photoresist pattern on the substrate.

NSMD pads
Short for Non-Solder-Mask-Defined pads, NSMD pads have solder mask openings that are larger than the pads.

pad
A small region of conductive pattern that is used for interconnections.

passivation layer
The protective layer which is deposited on the wafer at the end of the wafer fabrication process.

passives
Components such as resistors and capacitors that do not change state under the application of a voltage.

PCB
Short for Printed Circuit Board, a PCB serves as the structural base on which components are mounted. Conductive patterns on and within the PCB electrically interconnect the components.

PGA
Short for Pin Grid Array, PGA is a type of packaging that has area array pins that fit into sockets. Commonly used for the central processors of desktop computers.

photolithography
The technique of transferring patterns from a master template to a PCB/substrate by the use of light.

photomask
The template which contains an image of the circuit pattern to be transferred to the substrate. Light passing through the photomask chemically alters selected portions of a photoresist overlaid on the substrate.

photoresist
A photosensitive material which, upon exposure to light, becomes either resistant or susceptible to a chemical developer. Material remaining after development protects underlying layers from subsequent etching.

photovia
A microvia formed using photolithography

pick-and-place
The process in which components are placed onto PCBs before soldering.

pitch
The distance between adjacent interconnections.

plasma etching
A method in which tiny plasma fields are used to create holes in the copper and dielectric layers during microvia formation.

plasmavia
A microvia formed using plasma etching.

plastic packages
Packages with organic substrates and/or plastic molding encapsulant.

popcorn effect
The phenomenon whereby a package fails as a result of absorbed moisture expanding during heating.

positive mask
A mask which shields the desired circuit patterns. May refer to a photomask or the photoresist pattern on the substrate.

PTH
Short for Plated Through Hole, a PTH is a conductive hole passing through all layers in a PCB.

PWB
Short for Printed Wiring Board. See *PCB*.

QFP
Short for Quad Flat Pack, QFP is a package type that has peripheral leads arranged along all four edges of the package.

redistribution
The process of routing high-density circuitry to lower density circuitry.

reflow profile
The set of temperatures that the PCB and components are subjected to during board assembly.

reflow soldering
The board assembly process in which the solder paste that holds the components to the PCB is melted to form soldered interconnections. Also used as a general term describing the remelting of solder that has been previously deposited on pads, be it at the first or second level of interconnections.

screen
A taut metal mesh with exposed areas corresponding to the patterns to be deposited.

singulation
The division of a wafer into individual chips.

SIP
Short for System-In-a-Package, SIP describes a package which contains several chips (such as memory and processor chips) which make up an entire electronic system.

SMD pads
Short for Solder-Mask-Defined pads, SMD pads have solder mask openings that are smaller than the pads. SMD pads should not be confused with "Surface Mount Device".

SOC
Short for System-On-a-Chip, SOC refers to the integration of functions of several components onto a single chip.

solder joints
Interconnections which are made entirely of solder.

solder paste
A paste, containing solder particles, flux and solvent, that is used in the attachment of SMT components to a PCB.

SLC
Short for Surface Laminar Circuitry. See *build-up board*.

solder mask
The final layer of a PCB that serves to prevent unwanted deposition of solder on the PCB.

solder profile
See *reflow profile*.

solder resist
See *solder mask.*

stencil
A metal sheet with a circuit pattern cut into it.

stencil or screen printing
The deposition of material through openings in a stencil or screen.

substrate
A general term for a base.

subtractive process
The process of forming circuit patterns by selectively removing material from an initial full layer.

surface mount technology
The collection of techniques that allow components to be mounted onto the surface of a PCB.

TAB
Short for Tape Automated Bonding, TAB is the process in which the chip is attached to a polymer tape material before being attached to the substrate.

thermal cycling
An accelerated test method of subjecting devices to cycles of heating and cooling. Used to mimic the on and off cycles of an electronic device.

thermal profile
See *reflow profile*.

thin film
A layer of material that is built up by controlled deposition of individual atoms or molecules in processes such as chemical vapor deposition, sputtering or evaporation.

THT
Short for Through-Hole Technology, THT refers to the mounting of components on a PCB by placing their leads or pins into holes in the PCB.

trace
A conductive patterns on or within a PCB or substrate.

TSV
Short for through-silicon via, an interconnection which is essentially a plated hole running through the entire thickness of the silicon die. TSVs allow very high interconnection densities and high performance due to their short lengths.

UBM
Short for Under Bump Metallisation or Under Bump Metallurgy, the UBM is composed of several metal layers and serves as the interface between the upper layer of the die and the flip chip bump.

underfill
An underfill encapsulant is used to fill the spaces between flip chip bumps so as to reduce the stresses in the bumps during thermal cycling.

via
See *PTH*. Also a general term for a conducting hole.

wafer
The thin slice of semiconducting material on which numerous chips are fabricated.

warpage
The dimensional deviation of a substrate from a flat plane.

wave soldering
The process in which THT packages are soldered onto PCBs. During wave soldering, the bottom of the board comes into contact with a flow of molten solder.

wire bonding
The process of connecting the pads on a chip to pads on a substrate using very fine wires.

WLP
Short for Wafer Level Packaging or Wafer Level Package, WLP involves packaging the die at the wafer foundry.

Appendix E References

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